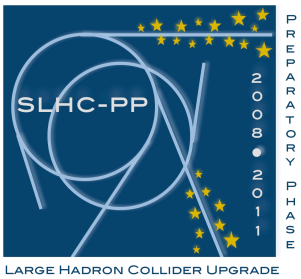

SLHC-PP

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EXECUTIVE SUMMARY

This report describes the LLRF prototype system which has been used to determine the field flatness during pulsed operation of a superconducting RF cavity in the test stand at CEA Saclay. The initial prototype system was built by modifying CERN's existing Lowlevel RF controls boards built for the LHC accelerator and operating at 400.8 MHz to cater for the required frequency of 704.4 MHz for the Lowlevel RF tests in the scope of the sLHCpp project. Following the experience during the cold tests on a cavity, a new Lowlevel RF board has been developed and is in production. It will be used for the final validation tests foreseen to be carried out on a cold cavity as part of deliverable 7.2.4 of the sLHCpp program. The advantage of the new Lowlevel RF board now in production is that it combines many functionalities that are spread over several electronic boards in the LHC system, onto a single board, thus offering a cost effective solution for a LINAC project employing some 200 individual cavities and RF stations. It also features functionality that can be used to condition the cavity.

Prototype Low Level RF system

1. STAND-ALONE MEASUREMENT SYSTEM

In the first phase of the project a stand-alone measurement system capable to measure the behaviour of a super conducting cavity under various operating modes was designed and built. A fully digital system allowed to do measurements with a high accuracy, and log the measured data for further analysis.

As a starting point a set of LHC LLRF hardware [1] was modified to SPL RF frequencies (704 MHz) to obtain a prototype measurement setup. The LHC RF system was already designed to be fully digital, based on VME bus technology. The VME crates are customized to have additional functionality required by a specific application. The special VME crate features a backplane with a standard type J1 (upper connector). The J2 connector (bottom one) is not used sacrificing the use with a 32bit data bus and 64bit address bus. Instead a custom Low-Level RF backplane is used for RF signal and timing distribution. Additionally the custom backplane distributes power, such as +/-6V, +/-12V for analogue electronics. Reference clocks are distributed up to 40 MHz using differential ECL, and 11 user triggers provide a possibility to trigger acquisitions and synchronize actions in the FPGA. A JTAG chain through all modules enables to remotely re-configure and program the FPGA on the individual VME boards.

The crate is controlled by a power-PC processor card inserted into the left most slot of the VME crate. The processor card has no non-volatile memory and needs a higher level control system to boot from the network (Ethernet). In the test-setup developed for the sLHCpp project a stand-alone computer was used with a network connection to the crate in order to perform the boot-operation and do the data logging.

Operational frequencies used in the LHC system are RF - 400.8 MHz, LO for all RF signals equal 19/20*RF i.e. 380.76 MHz and beam synchronous clocks of 80.16 MHz, 40.08 MHz and 20.04 MHz [2]. These were modified as described below in order to work at 704 MHz for the tests in the framework of the sLHCpp program.

1.1. COMPONENTS OF THE PROTOTYPE SYTEM

The LHC type crate used for the SPL tests was equipped with a “clock generator” module, a “LHC tuner” module, a “clock distribution” module and a “crate management” module [3].

The “Clock Generator” module receives a signal at the SPL RF frequency f_{RF}=704.4 MHz from a reference oscillator and generates, in the LHC so called, beam synchronous clocks – f_{RF}/10=70.44 MHz, f_{RF}/20=35.22 MHz and f_{RF}=17.61 MHz. The LO frequency f_{LO}=39/40*f_{RF}=686.79 MHz is also generated. The LO is used to mix down the RF signals to an f_{IF} of 17.61 MHz. The IF frequency is generated by a PLL which was designed to have a relatively narrow lock-in range. If needed a small deviation from the RF frequency is possible (if the cavity is not on tune), however for larger deviations (>1 MHz) correct functioning of the PLL must be checked prior to any operation or measurements employing this system.

The “LHC Tuner” module has four RF inputs [3]. These are mixed down to a fixed f_{IF}=17.61 MHz and then sampled by four fast, 14 bit ADCs at a sampling rate of f_S=4*f_{IF}= 70.44 MHz. The maximum input level of all RF inputs is around 0 dBm. The VME card is

equipped with 256 kWords of observation memory for each channel. The data are stored in form of an IQ pair, hence a total record of 128 k 14-bit samples per channel is available. The FPGA can reduce the sampling rate by decimation in multiples of powers of two, from the full rate of 35.22 Msps (record length 3.7 ms) down to about 1 ksps yielding a maximum record length of 127 seconds.

A stand alone Linux computer provides control and boot via Ethernet. An auxiliary second Ethernet port of the Linux machine can be used to connect a laptop or other computer to collect and analyze the data.

1.2. USAGE AS MEASUREMENT SYSTEM

A block diagram of the measurement set-up is shown in Fig. 1.

The signal from the reference oscillator is amplified and fed to the cavity. The directional couplers are providing samples of the Klystron forward, Cavity forward and Cavity reflected signals. The Cavity antenna signal is connected directly to the Tuner VME module.

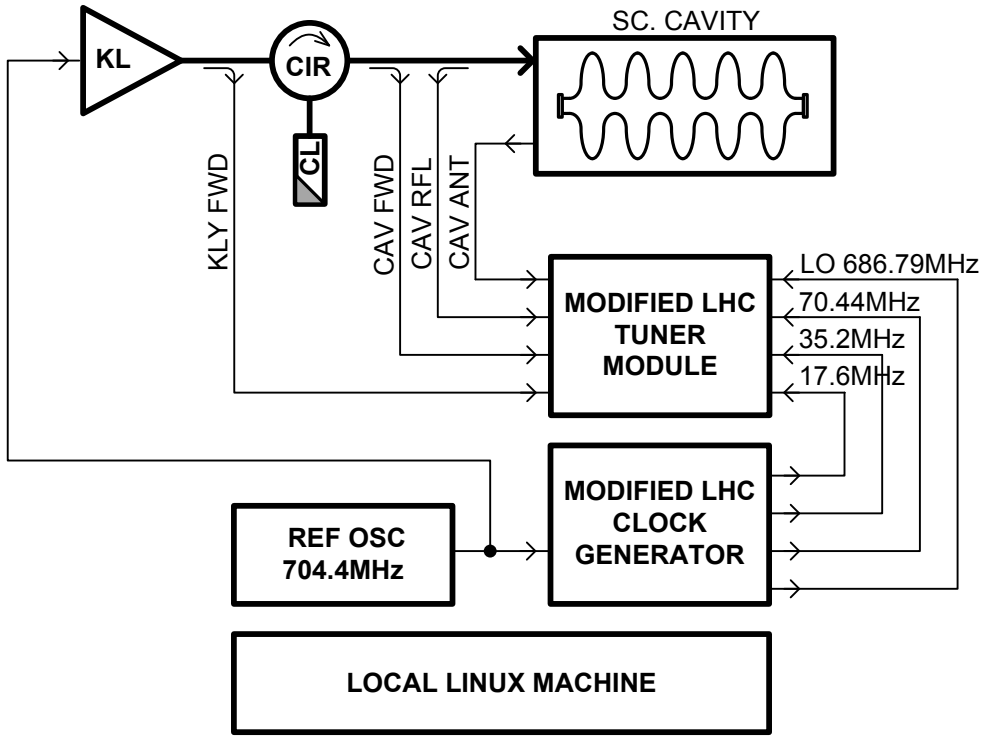

Fig. 1: Measurement set-up

1.3. LAB MEASUREMENTS ON A MODEL CAVITY

As a proof of principle a set of measurements were done on a model cavity in the Low-Level labs at CERN [4]. The actual measurement set-up is shown in Fig. 2.

The klystron was simulated by an RF power amplifier (27dBm out power), a circulator is not used and a small pin diode switch was used to pulse the incident RF signal. A simple model pillbox cavity was used instead of a super-conducting cavity.

The cavity frequency response is shown in the Fig. 3. It has a center frequency of about 707 MHz, and quality factor of about 20'000. The coupling antenna used makes the cavity slightly under coupled.

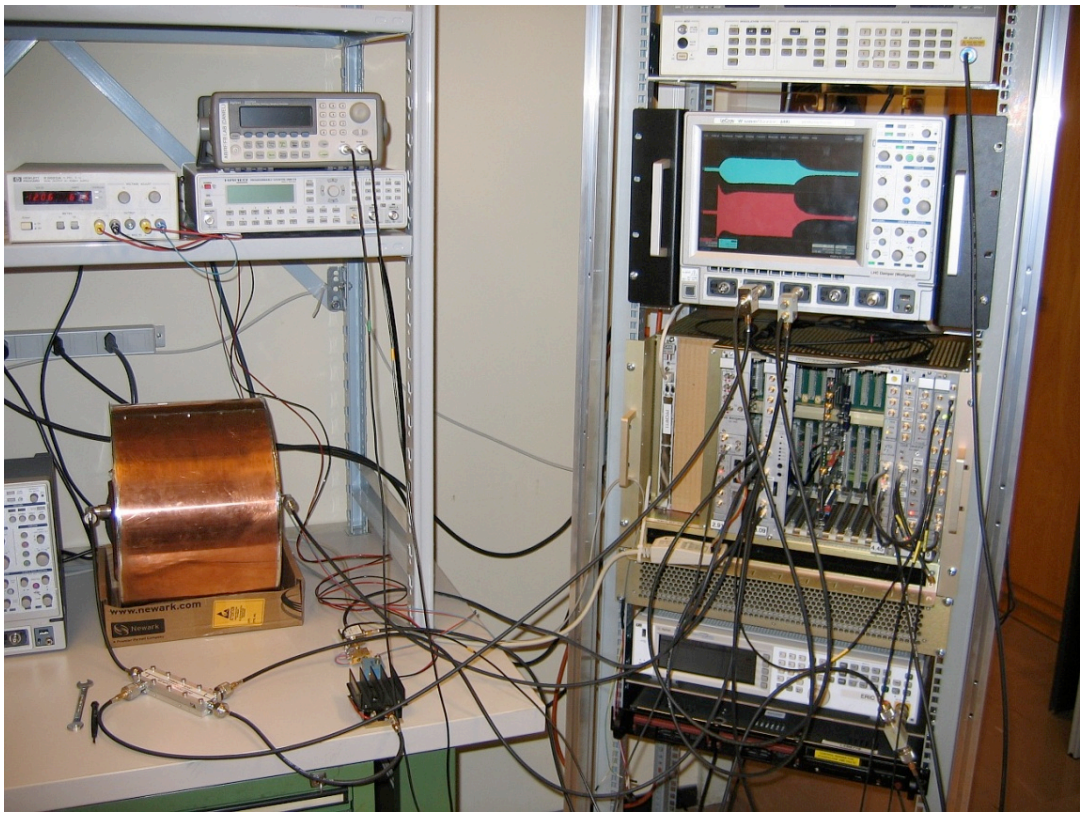

Fig. 2: The test setup in the LLRF lab at CERN.

The following picture shows measurement on the test cavity, namely cavity filling transient, cavity detuned by a fraction of a bandwidth. The four observed signals – Klystron forward, Cavity forward, Cavity reflected and Cavity antenna are plotted as vectors as a function of time (sampled signals). Amplitude is shown in the left column plots and the phase in the right column. The Klystron forward signal is taken from the reference oscillator before the RF switch in order to have a stable phase reference for the measurements.

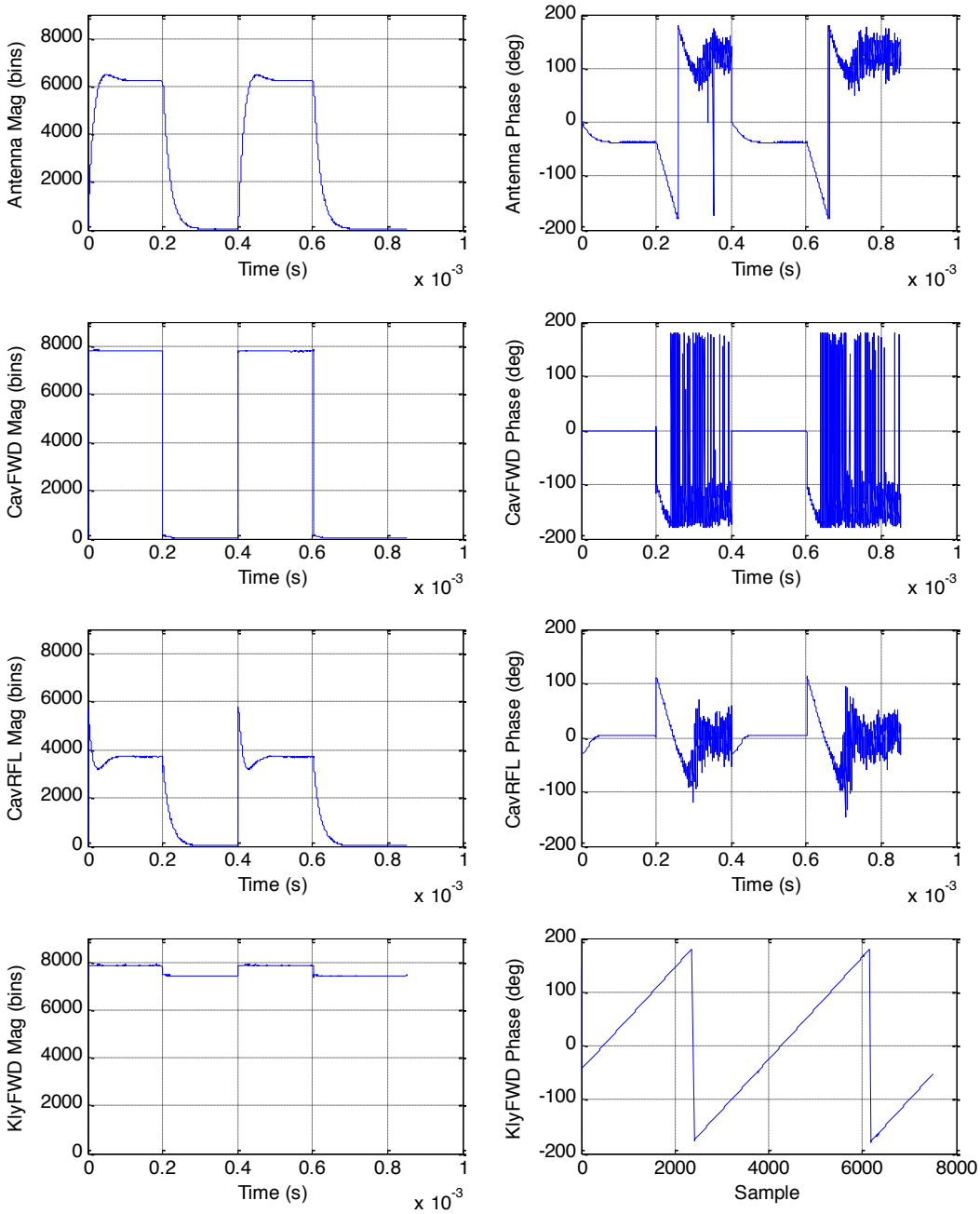

Figure 3: Cavity filling transient, cavity detuned by a fraction of a bandwidth, calibrated and corrected data

The measurement setup was transported to CEA Saclay CryHolab where it is being used since 2009 to test and qualify superconducting cavities. Results were presented at a LLRF workshop [5].

2. PROTOTYPE LOW-LEVEL RF SYSTEM

Based on the modelling [5] and measurements of the CEA and INFN cavity a prototype low level RF system was designed and built.

Typical RF system for a linear accelerator contains a large number of RF structures, powered either individually by a number of power RF amplifiers, or several structures powered by a single high power RF source. The field in each cavity needs to be controlled with a high level of precision requesting sophisticated control loops around each RF station. In case of the future SPL there would be some 200 cavities. Therefore the low level RF system must not only implement all required control functionality, but it also needs to be optimized for a large scale production and a very high level of automation for each task is essential (e.g. setting up, surveillance, trouble shooting etc.).

The proposed and designed prototype low level RF system is fully digital, based on a VME form factor. The system profits very much from the experience gained in the LHC construction and operation. Therefore the prototype LLRF system is built in the VME standard (for the hardware) and uses the FESA control infrastructure [6].

Unlike in the LHC or other synchrotrons at CERN, where the cavity controller and the low level system spreads over several VME cards or even several crates containing many VME cards, the proposed SPL prototype system was integrated onto only two principal VME cards. First, the *RF front-end module* houses the clock generators, RF down converters and a vector modulator. Second, *Digital Board*, carries four fast analogue to digital converters, powerful FPGA with all control loops implemented, observation memories, two fast digital to analogue converters and a socket for DSP drop-in module.

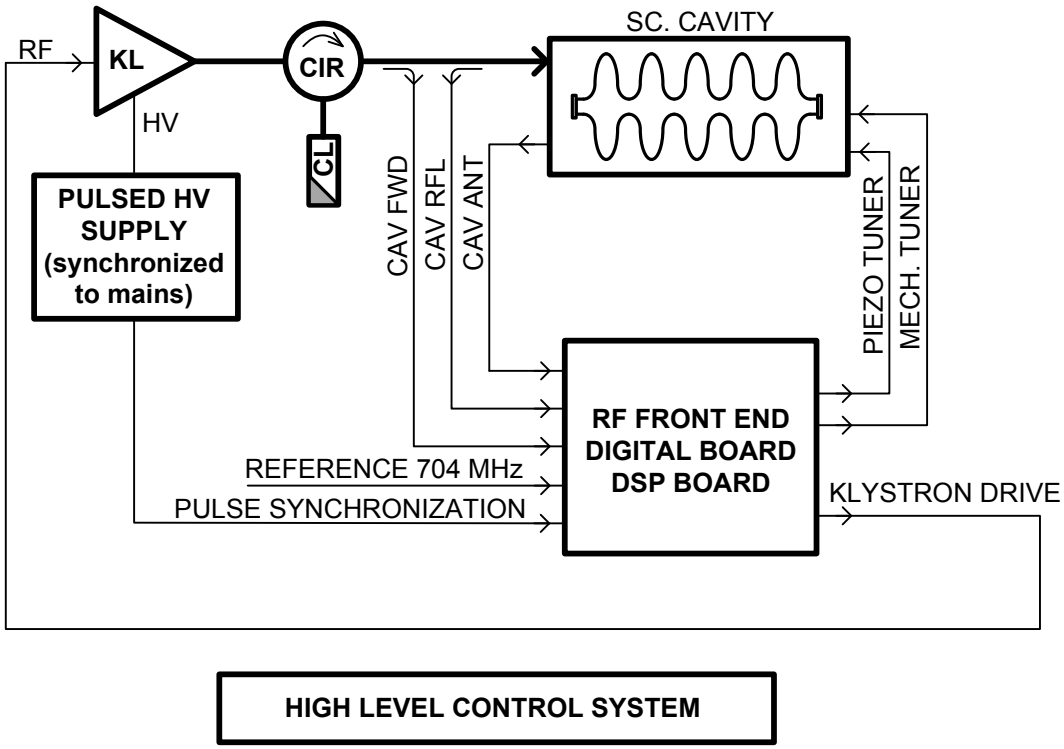

Fig. 4 Block diagram of the complete RF test installation

1.4. RF FRONT-END MODULE WITH CLOCK GENERATORS

The *RF front end module* was designed and optimized to contain all necessary analogue RF circuitry on a single board.

The RF front-end module down converts the complete set of four RF signals at 704.4 MHz (Reference, Cavity forward, Cavity reflected and Cavity antenna) to an intermediate frequency signals which are then sampled by four fast ADCs on the digital board.

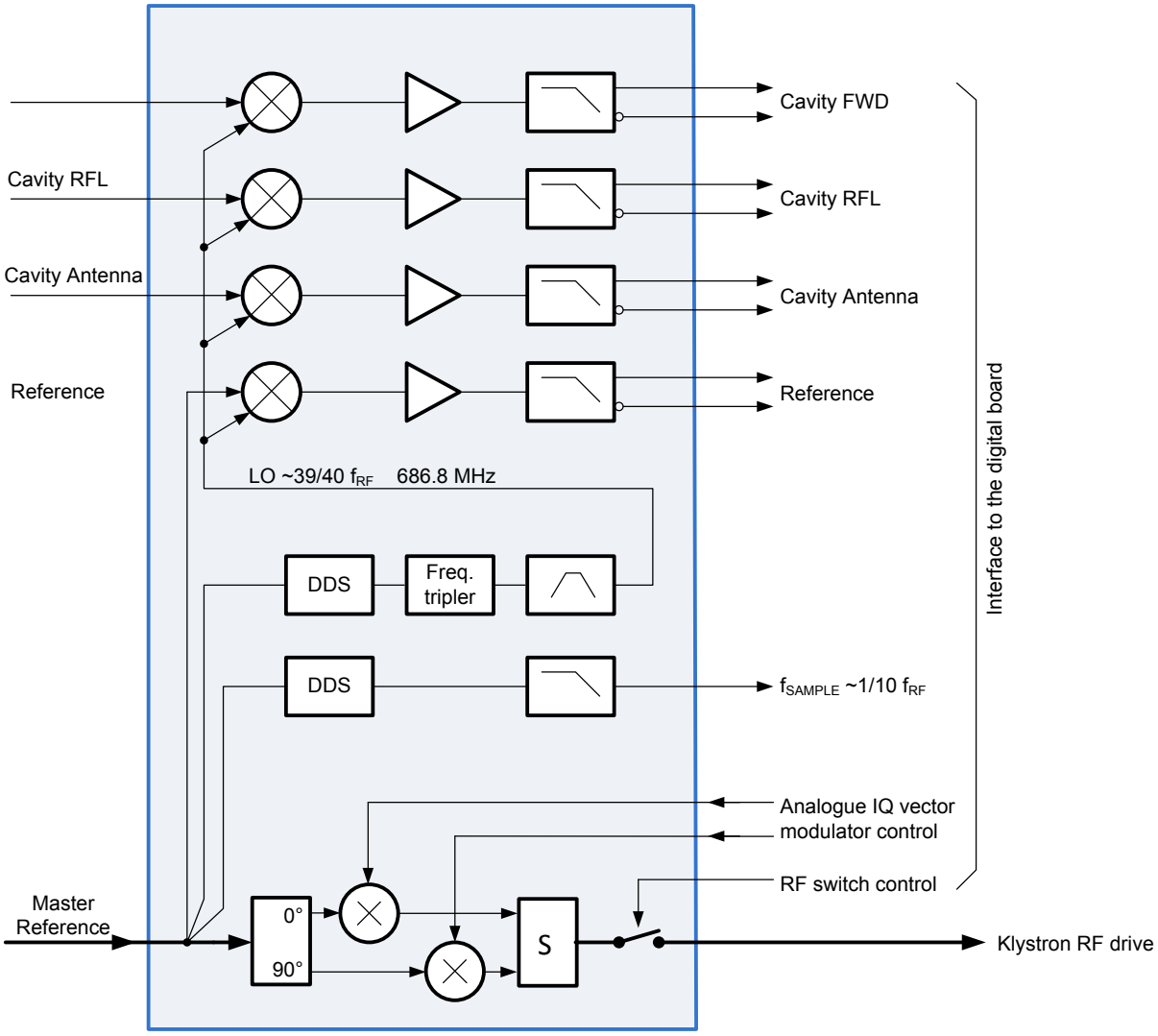

Fig. 5: Block diagram of the RF front-end module

A typical high speed ADCs providing reasonable bit resolution (12 to 16) and power dissipation (<2 W) used in various LLRF systems run up to ~ 100 Msps what is important parameter to define the feedback loop frequency and clocking scheme. The IF signals are sampled on the digital board using digital IQ demodulation technique with sampling frequency equal to four times the IF signal frequency. A convenient sampling frequency would therefore be $f_{sample} = f_{RF}/10 = 70.44$ MHz and intermediate frequency $f_{IF} = f_{sample}/4 = 17.61$ MHz. Corresponding local oscillator (LO) frequency is $f_{LO} = 39/40*f_{RF} = 686.79$ MHz.

The clocks are generated by two direct digital synthesizer (DDS) chips sharing the same RF reference. The sampling frequency $f_{sample} = 70.44$ MHz is generated directly by the DDS chip. The LO frequency $f_{LO} = 686.79$ MHz is too high to be directly generated by the DDS chip. Therefore a lower frequency $f_{LO*} = 13/40*f_{RF} = 228.93$ MHz is generated and multiplied to the final value of $39/40*f_{RF}$ by a frequency tripling stage.

All Reference, Cavity forward, Cavity reflected and Cavity antenna signals are mixed down to the IF using the same LO signal providing signals which are independent of absolute phase

relations between the LO signal and any of the four measured signals. Measurement stability is further improved by concentration of all critical RF circuitry on a small portion of the board where uniform thermal distribution could be assumed.

The klystron drive signal is generated from the RF reference by a means of an analogue vector modulator. The I and Q multipliers are controlled by two fast DACs located on the digital board. Vector modulator technique makes implementation of the control loops simpler, as the modulator is finally driven only by the error signals (either I/Q or amplitude/phase form). Use of the vector modulator also significantly simplifies implementation of the cavity conditioning system and klystron overdrive protection. Price to pay for simplicity is that the vector modulator has a limited dynamic range in amplitude control, typically 30-40 dB. If a wider amplitude dynamic range control is required later the vector modulator block could be replaced by an up convertor.

Finally, the output signal is gated by a fast high isolation RF switch.

1.5. DIGITAL BOARD

All control functionality is provided by one single module – the *digital board*.

In terms of hardware the board features 16-bit/100 Msps ADCs, an FPGA (Virtex4), and four static RAM memory chips of a total capacity of 2 Mwords as well as two 14-bit, 120 Msps DACs. The board has a connection to a commercial, off the shelf DSP evaluation board for the more demanding adaptive feedforward algorithms requiring floating point DSP functionality.

Four intermediate frequency signals (Reference, Cavity forward, Cavity reflected and Cavity antenna) delivered from the RF front-end module are sampled at $f_{sample} = f_{RF}/10 = 70.44$ MHz and sent to the FPGA feeding digital IQ demodulators. The demodulator provides one value of the RF vector at a rate of $f_{data} = f_{sample}/4 = 17.61$ MHz. This signal is used by fast RF feedback loops which require short loop delay (e.g. klystron linearization loop).

The required bandwidth of the cavity field loop is determined mainly by the very high Q of the superconducting cavity, and is of the order of 100 kHz or less [5]. The raw vector data are further decimated to reduce the loop bandwidth, lower the noise and obtain better regulation precision.

The Cavity forward and Cavity antenna signals are decimated to reduce the data rate down to few 100-ksps for the cavity detuning calculation. Pre-processing is done on the FPGA board and data is sent via a serial link to the external DSP board housing computationally demanding adaptive algorithm for the Lorentz force detuning compensation, driving the piezo actuator.

The FPGA board also houses the RF part of the cavity conditioning system. Using experience from the LHC, the conditioning algorithm employs the following: the control system sends short RF pulses with controlled amplitude and duration, while continuously monitoring the cavity “health” (vacuum rise, xray production). When given values are reached the pulse length and amplitude is increased and the process continues until the cavity reaches a fully conditioned state. Details of the implementation must be defined and adapted to the interlock circuits protecting the klystron and cavity. As the board is planned to be used at CERN as well as at the test facility at CEA Saclay with circuitry interfacing with the cavity and klystron interlocks will be flexible enough to be adapted to both cases.

Since all drive signals modulating the RF (loop output, conditioning signal etc.) are generated in the very same FPGA, the analogue RF chain does not have any additional inputs, it is possible to implement the “switch and limit” (SWL) controller directly into the feedback controller FPGA. Function of the SWL is mainly to protect the klystron and cavity from overdrive which can be caused by for example by an instability of the feedback loop, fast peaks, or incorrect set points asked by the control system.

Finally, the internal control signals are converted to the analogue domain by two 14 bit DACs feeding the analogue vector modulator on the RF front end module.

The board has several trigger input/output lines to synchronize with the machine timing system and the klystron power modulator. The design of circuit board has been completed and production of the board has started.

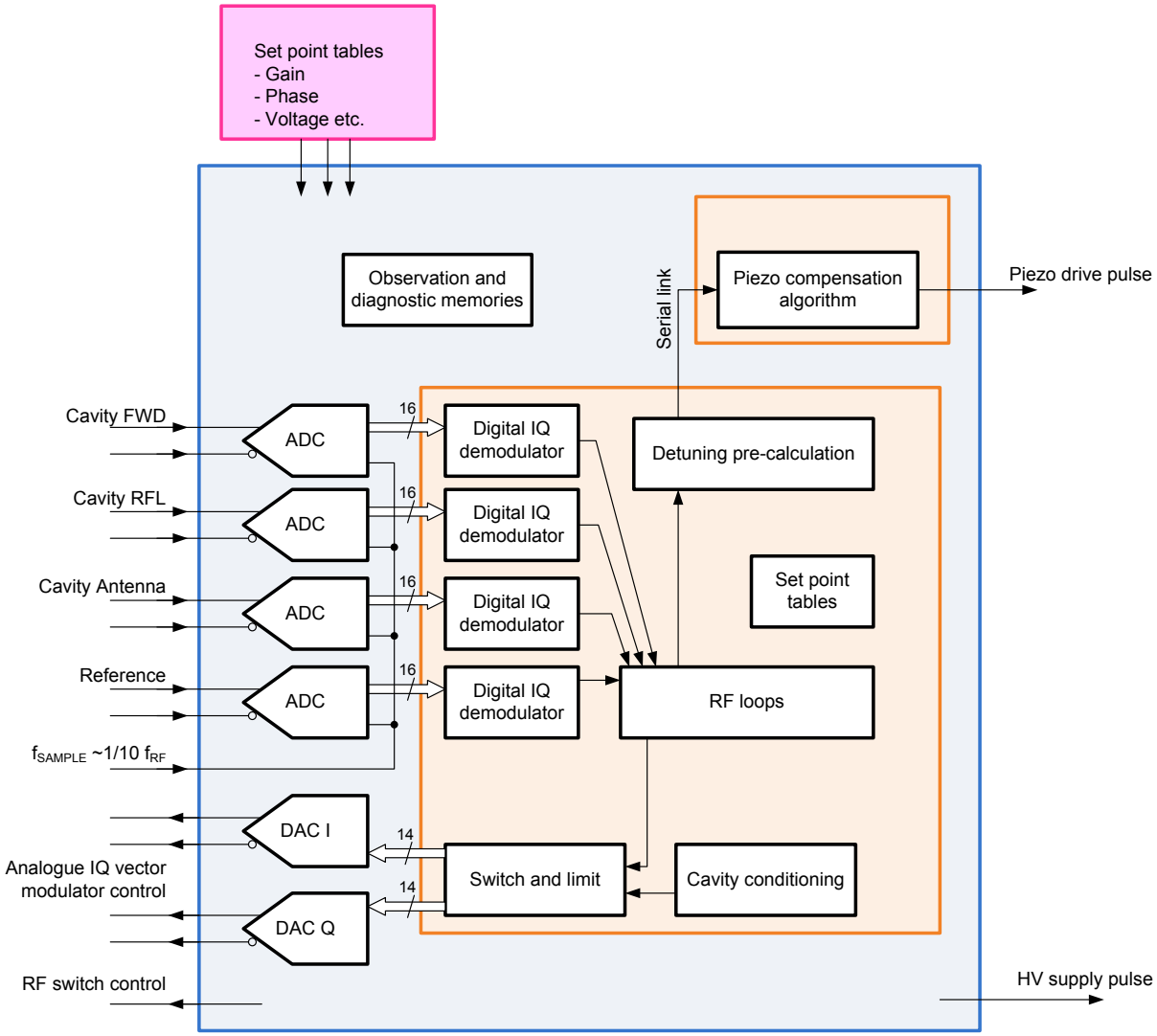

Fig. 6: Block diagram of the digital board

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