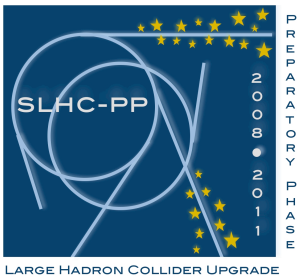

SLHC-PP

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1.1	16/03/09	Draft updated with Aachen results	K.Klein
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1.4	30/03/09	Final compilation with integration of suggestions from M.Weber	F.Faccio

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1. EXECUTIVE SUMMARY

In view of proposing a power distribution scheme for SLHC trackers based on the use of DC-DC converters, different conversion technologies have been studied in detail during the first year of activity. In particular, the impossibility of using ferromagnetic materials for the inductors in the large magnetic field in SLHC experiments, together with the low-volume and low-mass requirements for the converter, imposes strict boundaries to the usable technologies. After a research of the converter topologies typically used in commercial products and published in research papers, the study focused on five topologies potentially suitable for our application. The analysis of each topology allowed the development of a dedicated work sheet enabling the calculation of the current and voltage waveforms, and of the achievable efficiency. With this tool, the different topologies have been compared, and overall system efficiency for different configurations of converters (one versus two or more conversion stages) has been calculated. As a result, a power distribution scheme based on two conversion stages has been chosen as the most appropriate for SLHC trackers, and a topology has been chosen for each conversion stage: a buck converter for the first stage, serving a full detector module, and a switched capacitor voltage divider embedded on-chip for the second stage. A detailed study of this latter topology, with circuit-level simulations and optimization for powering the CMS pixel readout ASIC, has been done.

In addition to the above results, which fully meet the objectives set for the first year of activity, good progress has already been made on system integration issues. In particular, the installation of switching converters inside the trackers introduces an additional source of noise in a very sensitive environment. Switching noise from the converters can couple to the detector readout electronics through the electromagnetic field emitted by the converter's inductor, or it can be conducted via the power cables. To understand and limit the first noise path, a systematic study of the magnetic field emitted by air-core inductors of different designs has been carried out with the help of a simulation tool. This revealed how, to decrease the emitted magnetic field at close distance from the inductor, it is necessary to integrate an appropriate thin aluminum or copper shield. An inductor design allowing for easy and reliable integration of such shield is being explored. For what concerns conducted noise, investigations started with the design and assembly of a dedicated measurement station providing known impedance for common mode currents over a wide range of frequencies. Two very similar stations have been developed, at CERN and RWTH, enabling comparable tests at the two laboratories. These have been used to evaluate the noise of converter prototypes built using commercial discrete components, to decrease it with the use of appropriate layout and passive components, and to correlate system-level noise measurements on detector modules with the specific converter's noise.

The study of the system-level implications of the converters' noise has been performed on available detector modules/systems of the LHC generation (spares or prototypes of the systems installed in the LHC trackers). Full modules of the TOTEM silicon strip detector have been used to study the impact of the magnetic field emitted by an air-core inductor on the system noise. These modules showed small or negligible performance penalty when powered by relatively noisy converter prototypes. On the other hand, measurements on partially populated petals of the CMS Tracker End-Cap detector evidenced how the modules used in this system are rather sensitive to the conducted and radiated noise created by the prototypes. It appears hence that noise performance depends on the detailed implementation of the system, which determines its level of immunity to noise. The available detector

modules/systems are a precious tool to study this aspect, and will be further exploited to guide the design of new systems and of converter prototypes, and of their integration.

2. INTRODUCTION

In the design of upgraded trackers for SLHC, the HEP community will strive to further reduce material budget while at the same time increasing the number of detector readout channels. A quick look at the relative contribution to the total material inside the present LHC trackers clearly shows that cables and cooling systems are amongst the three main contributors – the third being the mechanical supporting structure which is also somehow related to the other two. Since both cables and cooling depend on the amount of power burnt in the tracker, there is the evident need to manage such power: how to minimize the power necessary to perform the electronic functions required inside the trackers and how to bring this power where it is needed.

To address the first issue, designers of Front-End (FE), control and communication electronics will optimize their designs to perform the essential functions at minimum power. This is efficiently achieved by a decrease of the supply voltage, implying the distribution of power at different voltages for digital and analog electronics functions. Analog readout circuits will in fact require the nominal voltage of advanced CMOS processes (1.2V in 130nm), while digital circuits will be able to function correctly with reduced voltage (0.9V). Additionally, optoelectronics devices embedded in the detector will require a supply voltage of 2.5V or above, actually increasing the power domains for the distribution system.

The number of power domains is not sufficient to draw a specification for the power distribution system without an estimate of the required current. Although the design of FE readout circuits for SLHC trackers is still in a very preliminary phase, a projection based on available estimates for the ATLAS tracker has been made. Compared to the LHC tracker now functional in ATLAS, the current to be provided to the load is expected to increase by a factor of 6. Since the power lost in a cable is proportional to the square of the current, this implies a 36-fold increase in losses if the power distribution system remains the same as today.

It clearly appears that, to be efficient, the new distribution system has to achieve a large decrease of the current in the cables from the power supplies (off-detector) to the hybrids, and has to support the distribution of different voltage domains. The use of on-detector DC-DC converters has the potential to meet these requirements, provided converters able to reliably work in the radiation and magnetic field environment can be developed. On-detector voltage conversion would indeed enable the desired reduction in current along the cables connecting the power supplies to the on-detector electronics. Such scheme is also capable of locally providing different voltage levels through the integration of different converters.

The aim of Work Package 8.1 is to develop and integrate radiation and magnetic field tolerant DC-DC converters for SLHC trackers. Since a large variety of conversion techniques exists, the main objective of the first year of activity was their detailed study and choice of the most appropriate one for the specific application in SLHC trackers in view of proposing a power distribution scheme. System-level issues related to the final integration of the converter in detector modules have been studied as well this year, and this activity will continue and expand in the future.

3. COMPARISON OF DIFFERENT CONVERSION TECHNIQUES

After an analysis of the distribution systems used in present LHC trackers, contacts were established with developers of the readout circuits for the upgraded SLHC trackers in order to better understand new system requirements and compile approximate specifications for the converters to be developed. An important requirement is imposed by the presence of a large magnetic field, which translates in the necessity of the use of air-core (or coreless) inductors. This in turns means that the converters will have to work with limited inductance values (maximum of about 500nH) and therefore they should operate at high frequency (around 1MHz). From the current view of the SLHC tracker system, output voltage levels of 2.5-1.8V and output power up to 9W appear reasonable. Moreover, to achieve the required decrease in current from the power supplies outside the detector, an input voltage of 10-12V is adequate. With all these boundary conditions, and after a careful review of the conversion techniques in the literature, five topologies were selected and studied in detail.

3.1. BUCK CONVERTER

This topology, shown in Figure 1, is the simplest and the one making use of the smallest number of components, but at the same time it requires a large output capacitance for ripple cancellation and it functions with the larger RMS current in the inductor – not ideal for electromagnetic noise.

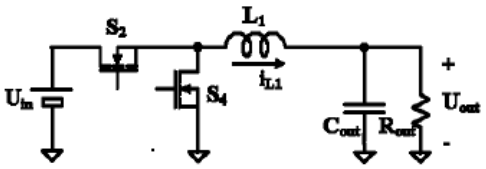

Figure 1: Topology of the buck converter

Two different design approaches can be followed: in the first, the converter is designed to operate in the so called “quasi square wave” mode (QSW), where each inductor current presents a high frequency ripple that is higher than twice its average value (i.e. the current goes negative for a fraction of each modulation period). In the second approach instead, the converter operates with relatively smaller current ripples in a typical Continuous Conduction Mode (CCM) condition.

The advantages of the first approach are represented, in the first place, by the reduction of the commutation losses. Indeed, high side switches’ soft turn on, of Zero Voltage Switching (ZVS) type, is achieved, as the inductor current turns the integral diode on before the switch. In addition, if the converter is properly designed, the turn-off of low side switches takes place at very low currents, practically achieving Zero Current Switching (ZCS), which leaves the turn-off of the high side ones as the only hard commutation (the turn-on of the low side switches is always soft, of ZVS type, in this topology). Therefore, switching losses are minimized. As a further advantage, the large current ripple calls for a smaller inductor value, as compared to the small ripple approach.

However, in the QSW mode, the increase of the inductor rms current negatively affects the conduction losses. In the small ripple, or CCM, approach there is no soft commutation, with the exception of the low side switches’ turn-on. On the contrary, the rms current on each inductor can be minimized, thus improving the conduction losses.

In general, a trade-off situation appears where the balance is favorable to the QSW approach every time the power switches present a reduced on-resistance which makes the switching losses dominant, to the CCM approach every time the conduction losses dominate. In our application, however, a further complication is represented by the limitation of the applicable inductance. Achieving CCM with a maximum allowed inductance typically requires the increase of the switching frequency, which, in turn, increases the switching losses. Therefore, although with the power switches typically available for fully integrated solutions, that present a relatively high on state resistance, the CCM approach could seem in any case preferable, the determination of the optimal approach is not so straightforward. To clarify the situation, a design sheet was developed by which, varying the critical parameters, an efficiency estimate was performed. The results indicated that for any given RDSon value (two possible CMOS technologies, with different transistor performance, were used), the maximum efficiency is expected to be achieved in the QSW mode of operation. The design sheet can be used to optimize the operation of the converter in terms of switching frequency and size of the transistors, a very useful tool in view of the final integration of the converter.

3.2. FOUR PHASE INTERLEAVED BUCK CONVERTER

The topology of a four phase interleaved buck converter is shown in Figure 2. The number of phases has been chosen to allow an ideally complete output current ripple cancellation at the required step-down ratio of 4 (10 to 2.5V). The principle of operation is based on the introduction of a quarter of period phase shift among the different phase commutations. This can be obtained by properly shifting the carrier signals in a four channel pulse width modulator. Operating at about 25% duty-cycle the converter achieves a significant reduction of the output current ripple, which, in turn, allows to: i) employ a reduced inductor value per phase, ii) minimize the output capacitor size, iii) increase the converter speed of response with respect to sudden load variations.

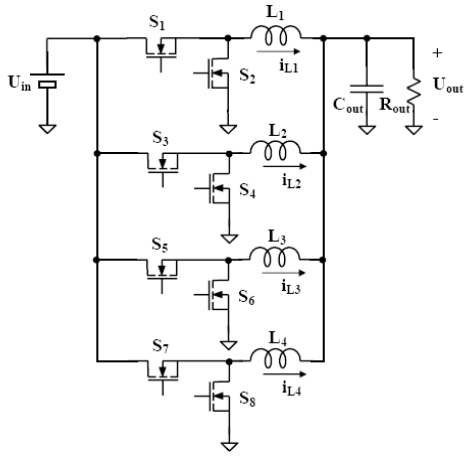

Figure 2: Topology of the 4-phase interleaved buck converter

Compared to the simpler buck topology, this converter requires a larger number of components and a more sophisticated control system.

As in the previous topology's case, it is not easy to identify the best design without a preliminary estimate of the efficiency. Again, a design sheet was derived for the 4-phase

interleaved buck converter and used to estimate the efficiency, as a function of the switch on resistance, the switching frequency and the inductor value. Also in this case, the best efficiency is achieved for QSW operation.

3.3. TWO PHASE INTERLEAVED BUCK CONVERTER WITH INTEGRAL VOLTAGE DIVIDER

The topology of the two phase interleaved buck converter with integral voltage divider is shown in Figure 3. As can be seen, the converter is derived from the standard two phase interleaved synchronous buck with the insertion of capacitor C1. The mode of operation is exactly the same of a two phase interleaved buck, with 180° shifted gate signals on phase 2 (switches S1 and S3, inductor L2) and phase 1 (switches S2 and S4, inductor L1).

Imposing the volt per second balance on both inductors, it is possible to verify that, for duty-cycles lower or equal than 0.5, the voltage across C1 is always equal to a half of the input voltage, independently from the particular duty-cycle or load conditions. The converter is therefore said to incorporate a voltage divider.

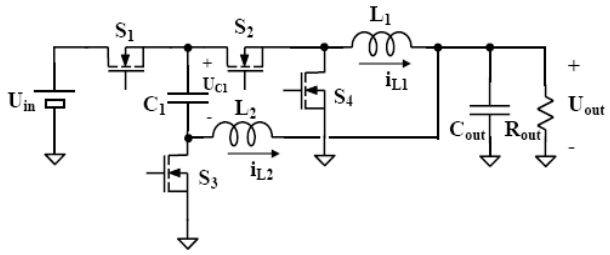

Figure 3: Topology of the two phase interleaved buck with integral voltage divider

The topology of Fig. 3 is interesting because, using only half of the active components and only two inductors, it gives the same conversion ratio as the four phase buck converter operating around a duty cycle D = 0.5 and so achieving an almost ideal ripple cancellation at the output. It is therefore possible to expect a lower volume occupation, because the need for an extra capacitor is likely to be over-compensated by the elimination of four switches and two inductors. In addition, the pulse width modulator complexity is greatly simplified as only two channels are required, one being 180° phase lagging the other.

As in the previous topologies' case, one could in principle choose conventional CCM operation or QSW operation. However, for this topology, the impact of the rms current increase determined by the QSW operation is expected to be relatively smaller, as the average inductor current is roughly twice that of the previous case.

As far as capacitor Cout is concerned, we observe that, in the steady state, the ac current across it is just the sum of the ac components of the inductors' currents and, as such, is subject to a partial cancellation effect, which helps to reduce the required capacitance.

Indeed, for D = 0.5 and in ideal conditions, a perfect current ripple cancellation can be achieved, which would allow to save the output capacitance altogether. However, when a residual ripple has to be filtered, the output capacitance must be inserted. The value can be fine tuned only by computing the residual ripple time integral, whose analytical calculation is not straightforward.

As for the previous topologies, it is not easy to identify the best design without a preliminary estimate of the efficiency. Again, a design sheet was derived for the converter of Figure 3 and used to estimate the efficiency, as a function of the switch on resistance, the switching frequency and the inductor value.

3.4. MULTI-RESONANT BUCK CONVERTER

This topology, shown in Figure 4 and originally proposed by W.A.Tabisz and F.C.Lee at the 1988 PESC conference, has the interest of reducing the switching losses because all switching takes place in either Zero-Voltage or Zero-Current conditions. Nevertheless, this comes to the price of having large RMS currents, hence large conductive losses, and large Vds across transistors – increasing the Vdd requirements on the technology. This is a problem for our application, where the wish for a fully integrated converter pushes us to the selection of CMOS technologies embedding high-voltage transistors generally limited to below 20V in drain-source voltage (while our design sheet of a multi-resonant converter with 10V input voltage indicates drain-source peaks up to 25-30V). Additionally, the resonance is found for a specific load condition only, and re-tuning is necessary for different loads – and our development aims at a converter applicable for a range of loads without major modifications. The design sheet developed for this converter topology also showed that, given the typical performance of transistors in the CMOS technologies targeted for the design, the efficiency of the multi-resonant converter is smaller than for the 3 topologies listed above.

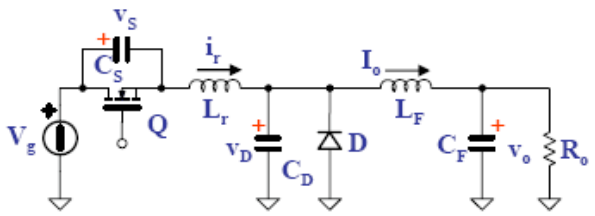

Figure 4: Topology of a multi-resonant buck converter

3.5. SWITCHED CAPACITOR VOLTAGE DIVIDER

This topology, shown in Figure 5, is the only one that does not require inductances, which is a nice feature given the limitations imposed to inductors by our application. The topology is relatively simple and so is the integration of this converter, and high-efficiency commercial implementations for a voltage division of 2 are available. A design sheet has been developed also for this converter, to estimate the efficiency and trade-offs between transistor and capacitance size and switching frequency. The results indicated that, for the power levels (up to 9W) and conversion ratio (higher than 4) identified for our application, it is very difficult to achieve high efficiency in a fully integrated design. Moreover, the output voltage regulation necessary in our application can only be achieved at the price of reduced efficiency.

The above considerations make this topology less attractive for the main power conversion stage, with input at 10-12V. At the same time, and because of the lack of inductors, the switched capacitor divider looks very attractive as a final divide-by-2 stage, embedded on the front-end ASIC, in a multi-stage distribution solution. Given the small level of current required

in this case (less than 100mA), high efficiency can be achieved with relatively small area occupation. This option has been the object of a dedicated activity and will be detailed in Section 7.

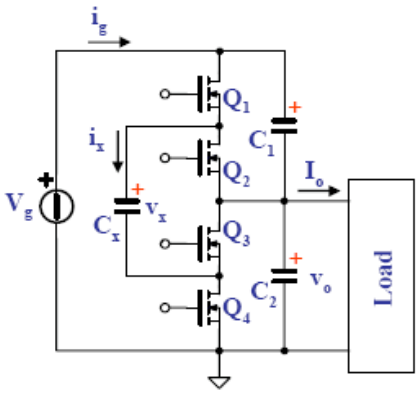

Figure 5: Switched capacitor voltage divider converter (ratio ½)

3.6. COMPARISON OF THE TOPOLOGIES

The five topologies have been compared for a conversion ratio of 4 (Vin=10V, Vout=2.5V) and an output power of 6W. For each topology, a study has been carried out to determine the current and voltage waveforms, hence estimate the different losses and eventually compute the efficiency. Calculations were carried out with Mathcad worksheets for each topology, making it easy to change the converter requirements (voltages, power) and the parameters of the inductor. The results are summarized in Table 1, where parameters for a 0.18μm high-voltage technology have been used and the switching frequency for the magnetic topologies was set to 5MHz – with the exception of the multi-resonant for which the frequency is determined by need for a resonant condition changing with the load and other parameters of the converter. For the switched capacitor solutions, 2 stages in series – each divide-by-2 – were used. It has to be pointed out that the results in Table 1 have been obtained without modeling in detail the switching losses; hence the obtained efficiency is optimistic for all topologies and should be used in for relative comparison only.

From the comparison table, and from the generic properties of each configuration listed above, it appears that the most appealing topologies are the simple buck converter (for its small number of components) and the 2-phase interleaved buck with voltage divider (for its efficiency, relative small number of components and complexity).

A more detailed comparison between these 2 topologies, taking into account all aspects (efficiency, noise, RMS currents), was necessary before a final choice could be made. To this purpose, the following actions were taken:

- Converter prototypes built with discrete components for both topologies were developed.
- A transistor-level simulation of the switching losses was performed using a CMOS technology embedding high voltage transistors, the one that most likely will be used

for the final integration of the converter. This element was poorly modeled in the worksheets used for the first efficiency evaluation.

- In-depth discussion took place with circuit designers involved in the development of the readout electronics for the upgraded SLHC trackers aimed at a more precise estimate of the power requirements. This led to a more accurate forecast of the output power from the converters, indicating a more limited budget of 2-4W.

Topology	Efficiency (%)	Freq. (MHz)	N. of switches	N. of caps.	N. of induct.
Buck converter	86	5	2	2	1
4-phase buck interleaved	88.3	5	8	2	4
2-phase buck interleaved with voltage divider	89.7	5	4	3	2
Multi-resonant buck	82.5	8.8	1	4	2
2 cascaded SW Cap	87.3	2	8	7	0

Table 1: Comparison of the 5 different converter topologies for Vin=10V, Vou=2.5V, Pout=6W.

The decrease in the foreseen output power of the converter, together with the transistor properties in the CMOS technology chosen for the final comparison, considerably decreased the efficiency gap between the buck converter and the 2-phase interleaved with voltage divider converter. In fact, the efficiency of both topologies increased with respect to the results summarized in Table 1, the two converters achieving a very comparable performance. Moreover, the conducted noise measurements of the two converter prototypes did not show a significant advantage in the noise performance of the interleaved topology. For what concerns the final converter's size, it was estimated that careful optimization of the inductors in both cases will lead to a similar overall area occupation. This is due to the fact that the 2-phase solution, which uses 2 inductors, can operate at the double frequency of the simple buck for the same efficiency, hence halving the required value for each inductor. Therefore the volume of the 2 inductors is equivalent to the volume of the single inductor in the simple buck.

Overall, the two topologies compared well in their performance and the decision in view of first ASIC prototyping was taken on the basis of the simpler design for the buck converter.

4. PROPOSED POWER DISTRIBUTION SCHEME FOR SLHC TRACKERS

Based on the results obtained by the review and comparison of different conversion techniques, a power distribution scheme meeting the requirements of ATLAS and CMS SLHC trackers was proposed. Such scheme is capable of decreasing the current on the cables from the power supplies and of locally providing different voltage levels through the

integration of different converters on the hybrid. This principle is shown schematically in Figure 6, where 2 step-down converters (thus named because Vout<Vin) are used along each power line. The first conversion stage on stave or hybrid provides 2 intermediate bus voltages: an “analog” 2.5V and a “digital” 1.8V. These buses locally run across one hybrid or a few neighbor hybrids. A second conversion stage, integrated on-chip, acts as a divider by 2 to supply the required voltage to the analog and digital circuitry on both the controller and readout ASICs. The overall conversion ratio achieved is close to 10, for a comparable decrease in the current on the 10V line coming from the off-detector power supplies.

A possible implementation of this scheme is shown in Figure 7, where a full stave is powered via a unique 10V line (the other line at the left of the stave is the optical link for communication purposes). At the left of the stave, one converter (stage 1) supplies 2.5V to the optoelectronics and the stave controller, where the required core voltage of 1.2V is generated on-chip by a conversion stage 2. In the case where the optoelectronics would require to be powered at 3V, this voltage could be generated by an additional conversion stage 1. Please note that in both Figure 6 and 7 the intermediate bus voltage is ideally divided by 2 on-chip, hence producing a 1.25V analog voltage, whilst in reality unavoidable losses will decrease it a little below this nominal value, making it closer to 1.2V. The same applies for the digital line.

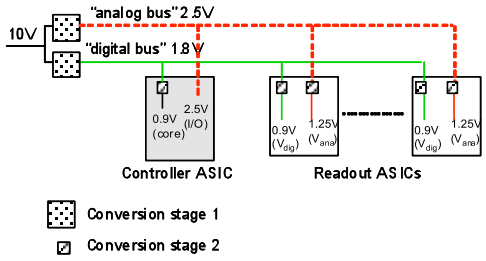

Figure 6: Power distribution scheme providing multiple voltage domains to the controller and readout ASICs from a single 10V line.

The main features of this implementation can be summarized as follows:

- Different voltage domains are generated locally from a single 10V line. FE analog and digital circuitry can be efficiently powered at the required Vdd.
- The current along the 10V line is decreased by a ratio of about 10 with respect to the load current. Power losses on this line are minimized ($P= R \cdot I^2$)
- The load current does not need to be constant in time. This is compatible with the presence of switching loads (for instance, for clock gating)
- The high modularity in the distribution of power allows for individual or grouped turning on/off of ASICs, greatly facilitating system start-up. In case of FE ASIC failures, individual groups can be turned off without loosing full hybrids.

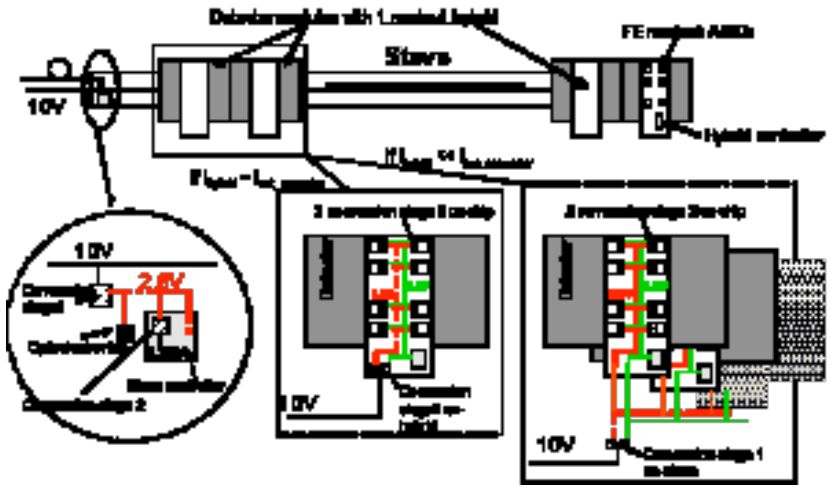

Figure 7: A possible implementation of the proposed distribution scheme. The choice on whether to have the conversion stage 1 on-hybrid or on-stave (to serve several neighbour hybrids) depends on the power rating of the converter and hybrid and on available space.

5. AIR-CORE INDUCTORS

The necessity of the use of air-core (or coreless) inductors has already been explained by the presence of a very intense magnetic field – up to 4T or 40,000 Gauss – in the tracker of the SLHC experiments. The ferromagnetic materials typically used in the manufacture of high-performance inductors for commercial converters saturate in such large magnetic fields.

A consequence of the lack of ferromagnetic core is a larger dispersion of the magnetic field created by the inductor when an alternate current flows in the device. Since this switching magnetic field can effectively couple noise in the sensitive detectors and associated readout electronics installed in close proximity of the converter (which is actually embedded in the detector modules, as shown in Figure 7), it is important to study its extension and magnitude and possibly find countermeasures to limit it. This study was performed with the help of two interactive software programs provided by Ansoft: “Maxwell 3D v11.1” and “Q3D Extractor”.

Maxwell 3D v11.1 is a package that uses the finite-element-method (FEM) analysis to simulate and solve three-dimensional electromagnetic field problems, basically processing Maxwell equations. Among several methods of analysis allowed by this software, the “Transient Solver” has been used to study the inductors; although it is slower and sometimes less precise than the “Magnetostatic” one, it is essential to evaluate the effect of a high frequency current into the inductor under test, taking into account also the inductive interaction between magnetic field source and surrounding elements (like ground plane and/or shields).

Q3D Extractor, instead, performs an electrical characterization of interconnected structures, such as those found in Printed Circuit Boards, providing values of capacitance, auto-inductance, DC resistance and AC resistance of all the involved components.

In order to study inductor performance in conditions as close as possible to those of their effective work environment, a sinusoidal current with 1 A peak and 1 MHz frequency has been chosen as input excitation for all the simulations.

The study focused on different designs for the inductor: solenoid or toroid. The former is by far the most common design for air-core inductors, with a large range of inductors (with different wire diameter) that can be purchased in the market.

Simulated radiation diagrams for a 150nH solenoid inductor are shown in Figure 8. All of them refer to the quarter period instant, which is when the injected current reaches the peak value of 1A, and therefore the maximum irradiation level (worst case evaluation). With the help of a graduated scale, it is possible to link the colors used in the graphs with the relative magnetic field induction level (all values greater than the maximum are represented by the same color of the maximum, that is red). The range of values taken into account is 1μT ÷ 15μT; this range allows us to study magnetic flux lines relatively far from the inductor (a few centimeters) but characterized by induction levels high enough to radiate effectively the surrounding area, potentially influencing other equipment placed in proximity. Higher levels of magnetic induction will, of course, be well contained inside the solenoid but they are not of our interest for what concerns the magnetic field irradiation. It clearly appears that the magnetic field extends sensibly outside the inductor, its magnitude being sufficient to inject noise in neighbor detector and electronics circuits.

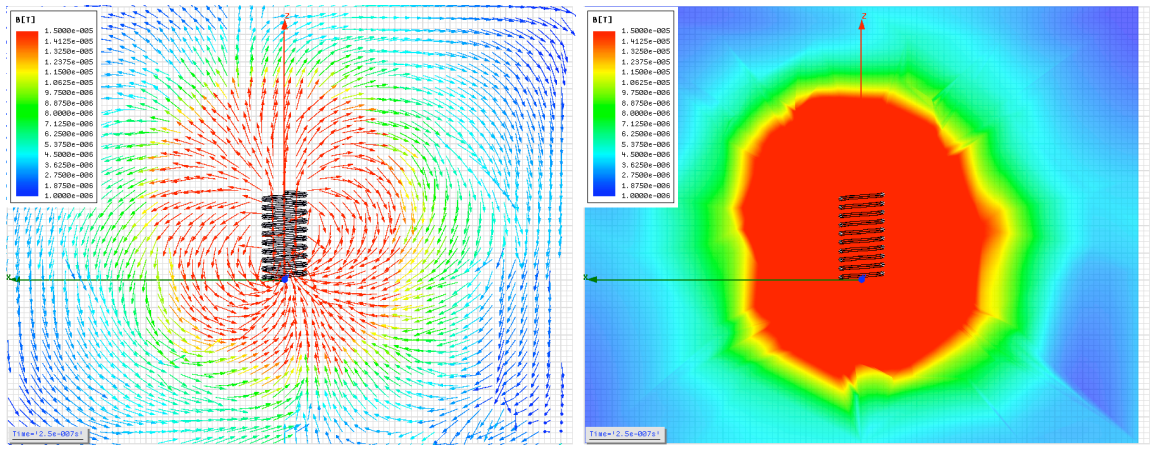

Figure 8: Vector (left) and magnitude (right) plots of the magnetic field around a 150nH solenoid inductor where a 1A current flows.

A toroidal shape for the coreless inductor should in principle contain the magnetic field inside the device, and the electromagnetic radiation in the surroundings should be well reduced. As shown in Figure 9, this is not really the case. If the magnetic field due to the coils is indeed contained in the toroid, there is nevertheless a parasitic field traceable to the one-turn loop of the current around the center of the toroid. As shown in the figure, and due to the relatively large diameter of the toroid, this field can reach levels comparable with those for the solenoid inductor.

From this study, it appears that a drastic reduction of the magnetic field in close proximity of the converter (actually, of the inductor used in the converter) can not be achieved simply with a specific geometry for the inductor, but with appropriate shielding. Efficient shielding at the switching frequency of the converter can be obtained with a thin layer of aluminum (less than 100μm). Study of the best inductor design enabling easy and practical shielding is under way.

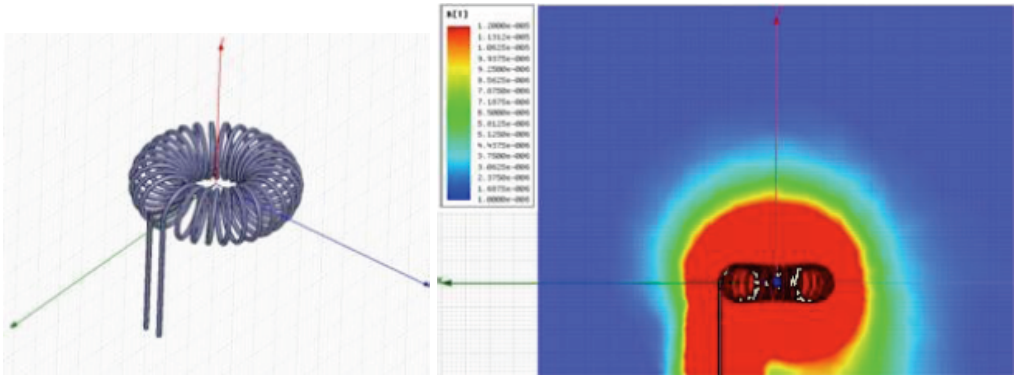

Figure 9: Geometry (left) and radiated field (right) for a toroid coreless inductor. The extremes in the colour scale are $1.2 \cdot 10^{-5}$ (red) and $1 \cdot 10^{-6}$ (dark blue)

6. TOWARDS INTEGRATION IN DETECTOR MODULES

The development of the converters has to take into account all issues related with their final integration in the full tracker system. While some of these issues will only be known at the time of prototyping SLHC-grade detector modules and staves, many others can already be explored and studied now, either with specialized measurement stations or by using detector modules/systems of the LHC generation (spares or prototypes of the systems installed in the LHC trackers). This section describes the activity that has taken place in this direction.

6.1. DEVELOPMENT OF SPECIALIZED MEASUREMENT STATIONS

Target DC-DC converters for our application are switching devices operating at MHz frequency and commuting nodes at high voltage (10-12V). This type of electronic devices is a potential source of conducted noise to the load – the front-end electronics to be powered by the converter – and also to the line from the main power supply. Amongst the different types of conducted noise, the most deleterious at the system level is common mode noise. Common mode noise currents flow in large loops where the return path is typically difficult to control. The size of the current loops makes this type of noise capable of large coupling to the surrounding equipment.

When developing DC-DC converters, and in view of a final low-noise implementation, it is important to be able to characterize the converter prototypes in terms of conducted noise emission. Common mode currents being directly dependent on the impedance of the return path, even small differences in the experimental setup can give completely different results for the same converter. It is therefore necessary to develop a reference test setup which presents well controlled impedance to the input and output lines of the converter prototypes over a large bandwidth. This is achieved with the use of Line Impedance Stabilization Networks (LISN). Additionally, circulating currents have to be measured with the help of current probes connected to a spectrum analyzer.

Two similar and cross-comparable measuring stations have been developed to this purpose: one at CERN and one at RWTH. Their schematic composition is shown in Figure 10. A picture of the CERN implementation is shown in Figure 11, while Figure 12 shows the set-up realized at RWTH Aachen University.

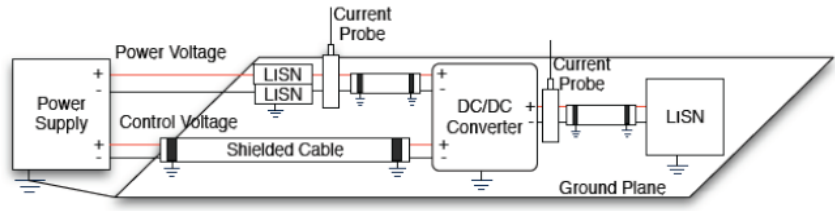

Figure 10: Schematic representation of the reference test station for conducted noise

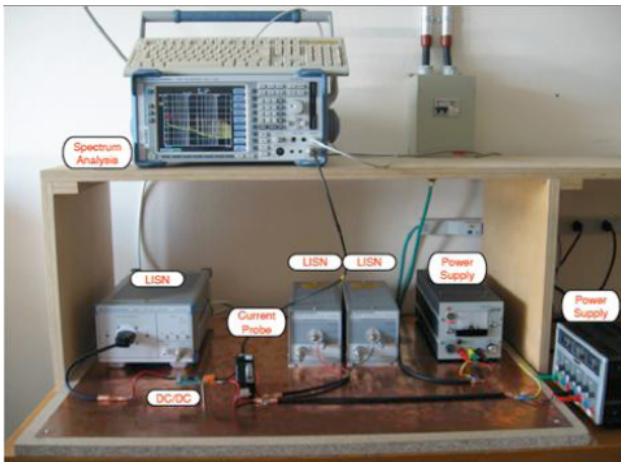

Figure 11: Reference tests station installed at CERN

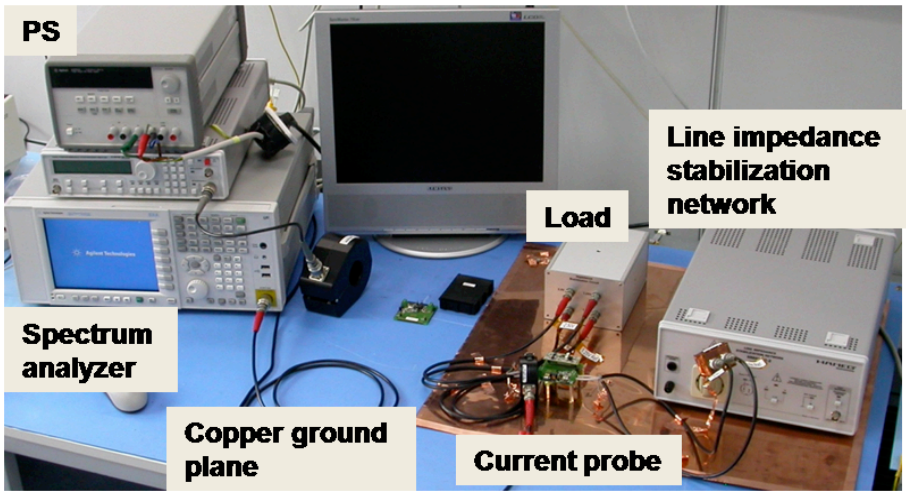

Figure 12: Reference test station installed at RWTH Aachen University

The dedicated measurement station has been used to evaluate the noise of different converter prototypes built using commercial discrete components. In this way, it was possible to measure directly the impact on the conducted noise of layout modifications and changes in the passive components used in the converter (capacitances). This led to the development of

a model for the noise sources in a converter, and to a considerable improvement in the conducted noise performance of the prototypes. As an example, Figure 13 shows the large decrease in output common mode noise from the second (left) to the third (right) generation of prototypes. It should be noted that both prototypes make use of the same controller and power switches, only the layout and passive elements have been modified.

At RWTH Aachen University the set-up was used to characterize various PCBs with commercial buck converter chips. These PCBs were developed at RWTH Aachen for system-test measurements with current CMS tracker substructures (Section 6.2.1). The reference test station allowed correlating changes in system noise with the Differential and Common Mode noise spectra of the converter boards.

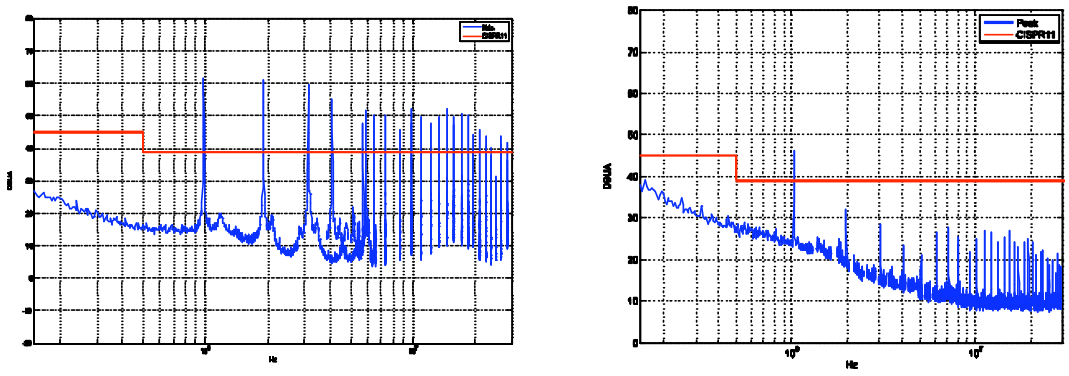

Figure 13: Output conducted noise from two converter prototypes with the same active devices (controller, power switches) but different layout and passives. The level of the peaks, at the switching frequency of 1MHz and all harmonics, are representative of the noise performance, while the red line is a reference guide for the eye – actually translated in current from the CISPR11 standard. The improvement in the performance of the prototype in the right figure is outstanding.

6.2. MEASUREMENTS WITH DETECTOR MODULES AND SYSTEMS

First measurements at the detector module level have taken place using existing hardware from the current LHC experiments. This activity took place at CERN, where measurements were performed on Silicon Strip detector modules developed for the TOTEM LHC experiment, and at RWTH, where measurements were performed on modules and partially populated full petals of the CMS TEC endcap detector.

6.2.1. Measurements on the CMS TEC modules

In the absence of any prototype structures for the CMS tracker upgrade, substructures of the current tracker end caps (TEC), referred to as petals, have been used for the system test. While future devices will be different in many respects, important lessons can already be learned from operating current tracker structures with DC-DC converters.

The test petal was equipped with four silicon microstrip modules. These modules carry two daisy-chained sensors with AC-coupled p-doped strips implanted in a 500 µm thick n-doped bulk. The sensor strip capacitance amounts to about 20 pF. The connections between sensors and between the first sensor and the FE-electronics are realized with wire bonds.

The FE-hybrid carries six APV25 readout chips, which are manufactured in a 0.25 µm CMOS process. Each chip processes the data of 128 channels. The read-out is fully analogue. For each channel, a charge-sensitive pre-amplifier, a CR-RC filter with a time constant of 50 ns, and a 192 cells deep pipeline are implemented. The data are sampled at 40 MHz. The APV25 is powered from two supply rails, namely 1.25 V and 2.5 V. Typical currents are 60mA and 120 mA, respectively.

All modules have been powered and read out during the measurements. The petal was equipped with the original motherboards (InterConnect Board, ICB). Both readout and digital signaling were realized optically. PCI-based prototypes of the readout, trigger and control cards have been used. The petal has been thermally stabilized at +15°C. It was housed in a grounded metal box. The set-up was very similar to test systems used during the integration of the CMS tracker.

Since custom radiation-hard DC-DC converters were not yet available when the tests were started, commercial buck converters were used instead. The first tests were performed with buck converters with internal coils. A market survey was performed to identify a device with high switching frequency, low conversion ratio U_{out}/U_{in}, a suitable output voltage range and sufficient output current. The Enpirion buck converter EN5312QI with a switching frequency of 4 MHz, a maximal recommended input voltage of 5.5 V and a maximum output current of 1 A was chosen. This device implements an internal planar inductor in MEMS technology. Two chips, configured to provide 2.5 V and 1.25 V, respectively, were mounted on a four-layer PCB, together with input and output filter capacitors and connectors. This PCB can be plugged between the ICB and the module. Two versions of the PCB have been tested: the L type (Fig. 14, left) is slightly larger, the S type (Fig. 14, right) is smaller and more modular in design, with a separate PCB for the connector.

The input power is supplied either directly from an external power supply or via the 1.25 V plane of the ICB. No difference in performance was observed between these options. In most measurements, the board was powered with 5.5 V directly from an Agilent E3633A PS. The raw noise (calculated as the RMS of the fluctuations around the pedestal value) distribution of one module is shown in Fig. 15 (left). The noise level is slightly increased by up to 10% w.r.t. measurements without DC-DC converters. The additional contribution is common mode (CM), defined as a common event-wise fluctuation of all strips of an APV25, and calculated as the median of the signals after subtraction of the pedestals.

With the S type board, the increase of noise is almost negligible. The difference between the boards has been traced back to the additional connection between the main and “connector PCB”. Clearly a careful PCB design is very important to achieve an optimal noise performance.

Edge strip channels are known to be sensitive to noise effects, such as coupling from the bias ring or common mode due to bad grounding. With converters, the noise on module edge strips increases by up to a factor of 10 (Fig. 15, right). Furthermore, the noise on disconnected channels increases from a low level to a level even above the mean. For the interpretation the common mode subtraction inside the APV has to be considered. Each APV channel implements an inverter stage. These are powered from 2.5 V via a common resistor, located on the FE-hybrid. If a common mode signal is present at the inputs of the inverters, a voltage drop is created across the resistor that drives down the inverter output and effectively subtracts the common mode from it. This, however, does not apply to channels which see a lower than normal CM, such as disconnected channels, or a higher than normal CM, such as edge channels. If a certain common mode is present in the system, the CM they see will be

overcompensated or not completely subtracted, respectively. Their signal is thus a sensitive indicator of the CM actually present in the system, and cannot be neglected.

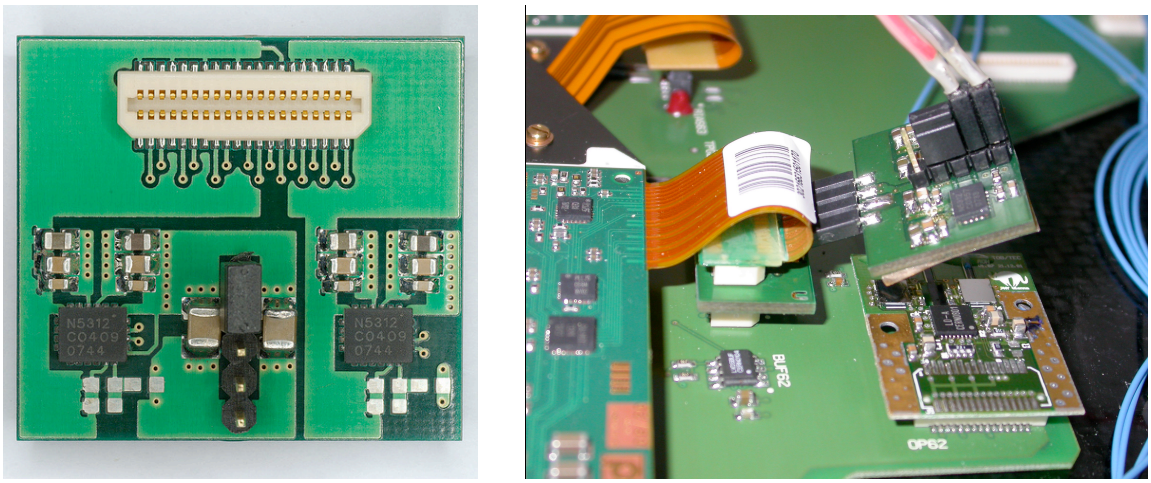

Figure 14: The converter PCBs: L type (left) and S type integrated onto the TEC petal (right)

To study potential cross-talk effects, the correlation matrix between all pairs of strips has been computed for two adjacent modules that were powered with converters. With ordinary powering, correlations amount to around 5% both for strip pairs within and between modules. With converters, correlations of 10-20% are observed for strip pairs within modules, reflecting the increased common mode. The correlations between modules are however not increased significantly, i.e. cross-talk between modules is not observed.

To investigate the potential effect of a Low DropOut regulator (LDO) on the voltage ripple and thus the noise, another PCB was developed. The LDO LTC3026 from Linear Technology was connected to the output of EN5312QI. A ripple rejection of around 45 dB for the switching frequency of 4 MHz is quoted in the data sheet. Tests were performed with dropouts of 50 and 100 mV. Already for a dropout of 50 mV, a beneficial effect is observed: the raw noise is no more increased and the noise on edge strips is only a factor of 2 above the normal level. This indicates that the noise in the TEC system is mainly caused by a conductive coupling of a differential mode component of the converter noise.

Since ferrite inductors cannot be used in the final experiment due to the high magnetic field of 4 Tesla, commercial buck converters have been equipped with external air-core inductors. For these tests, the Enpirion buck converter EQ5382D has been chosen, which is similar to EN5312QI, but has no internal inductor. PCBs similar to the L type have been fabricated and equipped with various coils: planar ferrite inductors (Murata, L = 1 µH), air-core solenoids (Coilcraft, L = 538 nH) and custom-made air-core toroids (L = 600 nH). With air-core inductors, the noise increases drastically compared to internal or external ferrite inductors. For toroids the increase is a factor of 2-3 lower than with solenoids. In Fig. 16 the noise distribution using toroid coils is shown (red curve). The edge strip noise increases enormously, up to about 90 ADC counts for solenoid coils. When a module was operated with an air-core coil, the noise increased also on its conventionally powered neighbour modules.

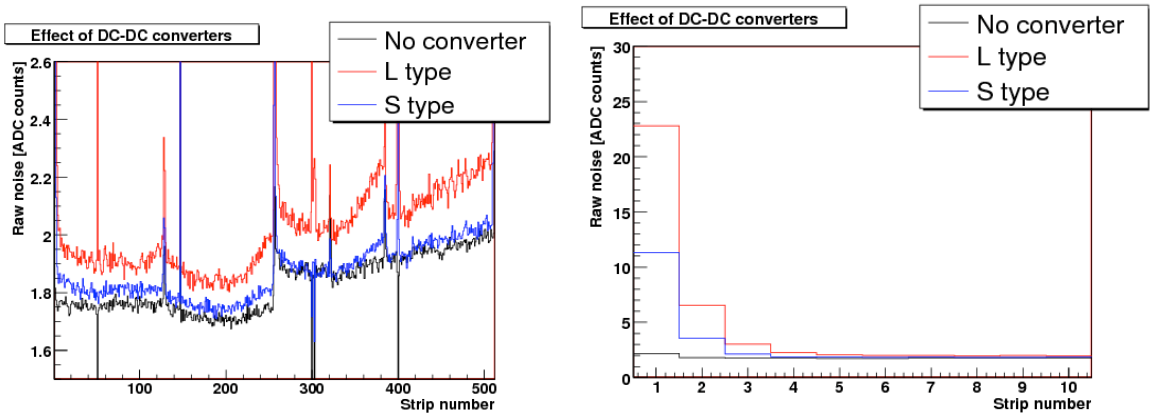

Figure 15: Raw noise (left) and edge strip noise (right) for conventional powering (black) and powering via L type (red) and S type (blue) DC-DC converter PCBs (red) and S type (blue) DC-DC converter PCBs.

The wing-shaped noise has been traced to a pick-up of radiated noise in the FE-hybrid region. This has been proven in tests where the module was powered conventionally but exposed to the radiation of noise by powered but unplugged converter boards or individual coils operated with a frequency generator. In both cases, wing-shaped noise was induced in the module.

Tests have been performed with shielded converters. The PCB was wrapped in copper or aluminium foil of 35 and 30 µm thickness, respectively. The noise decreased significantly (blue curve in Fig. 16). The noise contribution remaining with shielding is probably induced conductively. Studies of the material budget within the CMS software framework have shown that shielding the inductor with a thin aluminium foil could be acceptable.

The pink curve in Fig. 16 shows the combined effect of shielding and using an LDO regulator. The noise is very similar to the noise measured with conventional powering techniques.

Finally the distance between the converter PCB and the FE hybrid has been varied. The noise increase depends strongly on the distance. When the distance is increased by a few centimetres, the remaining increase of noise is almost negligible. An operation of buck converters on the substructure level could thus be preferred from the point of view of noise radiation.

The preliminary conclusion from the system test with CMS modules is that they are rather sensitive to the switching noise and radiated noise created by (commercial) buck converters, but that on the other hand effective counter-measures do exist. These must be further studied and exploited. The tests have also revealed that many of the features observed are related to the design of the current FE-electronics. Measurements with CMS silicon detector prototypes for SLHC will be conducted as soon as they become available.

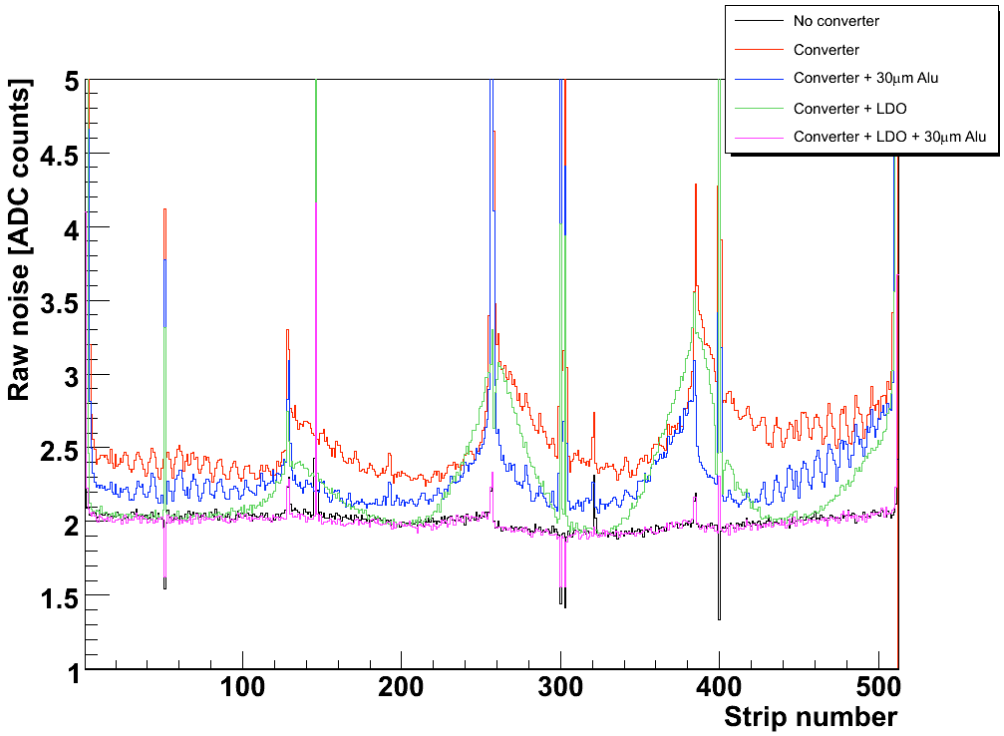

Figure 16: The raw noise distribution of module 6.4 with ordinary powering (black) and powered with a DC-DC converter PCB with an air-core toroid coil (red). In addition the effect of various measures to control the noise is displayed: with a thin aluminium foil used to shield the inductor (blue), instead using an LDO regulator (green), and finally the combination of shielding and using an LDO regulator (pink).

6.2.2. Measurements on the TOTEM modules

TOTEM is a silicon strip detector designed for luminosity monitoring. The front-end strips are coupled to a VFAT2 ASIC that shapes, amplifies and discriminates the strips signals. The discriminated signals are packed and transmitted by the hybrid board as LVDS signals. A test board allows testing the hybrids prior to their installation. The test system is controlled by a dedicated software tool that configures the detector and analyzes the transmitted data. In our measurements, the system has been exposed to electric and magnetic field sources with the aim to understand its compatibility with DC-DC converters located in close vicinity of the front-end ASICs.

As already mentioned above, a major concern when embedding DC-DC converters is the magnetic field emitted by the coreless inductor at the switching and harmonic frequencies that can introduce noise in the preamplifier inputs. Electromagnetic simulations carried out with Ansoft Maxwell and reported in section 5 above indicate that the magnetic field emitted along the axis of a coil decays very fast with the distance, being reduced by two orders of magnitude at 10 mm of the coil edge. To verify this, an inductor (Coilcraft 538 nH air core) was driven with a 0.5A, 1 MHz signal, pointing at different locations and angles around the front-end system as shown in Figure 17. At these locations and angles, the S curves parameters were evaluated by the test platform for every channel. The dispersion of the slopes is used to estimate the susceptibility to the magnetic field.

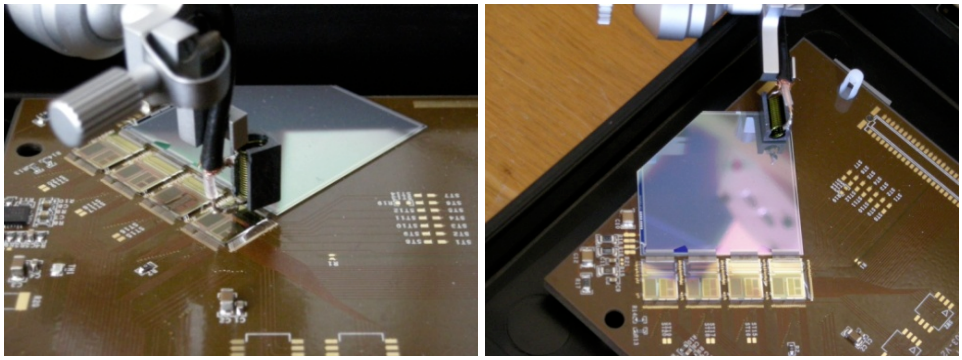

Figure 17: Measurements of the noise induced by a coreless inverter with alternating current on the TOTEM silicon strip modules.

The coupling between the coil and the strips indeed decays fast with the distance, becoming negligible beyond 20 mm. However, the coupling is strongly reduced by the addition of a shield, either around the coil (Al foil) or in the form of a copper plane above the sensitive area. This confirmed the necessity for shielding the coreless inductor.

Measurements on the noise performance of the TOTEM module were also made when powering it with the available prototype DC-DC converters built with discrete components. When the converter was positioned very close (less than 2cm) to the detector or VFAT readout chips, the noise of the silicon strips (channels) close to the inductor in the converter prototype increased by about 60%, whilst farer strips had nominal noise. This problem, traceable to the radiated magnetic field from the coreless inductor, can be solved with appropriate shielding of the inductor. On the other hand, when the converter was positioned farer than 2cm from the detector and VFAT chips, the effect of the conducted noise alone could be measured and turned out to be limited to an increase of less than 20% for a first prototype and no increase for another prototype. These results are very encouraging in view of the final integration of the converter in a full detector system.

7. ON-CHIP SWITCHED CAPACITOR CONVERTER (CHARGE PUMP)

To study charge pumps for powering the detector frontend electronics, a test structure was developed and a design realized in a 250nm CMOS technology. The implemented circuit is a 2:1 switched capacitor DC-DC converter. Figure 5 shows the principle of such a charge pump. In CMOS technology, the switches are integrated as NFET and PFET transistors. Figure 18 shows the detailed schematic of the implemented circuit. To drive the gates of the four transistor switches, three driver stages are needed which are optimized for speed and exact timing. To switch between the two states a non overlapping two phase clock is needed. This is generated by a dedicated circuit. All these components are implemented on chip. The capacitors are external because it is not possible to place the needed capacitance values in the nF (10^{-9} Farads) range on the chip. The clock generator is external too because in the application the LHC machine clock will be available and it will be hence possible to use it to generate the required clock signal.

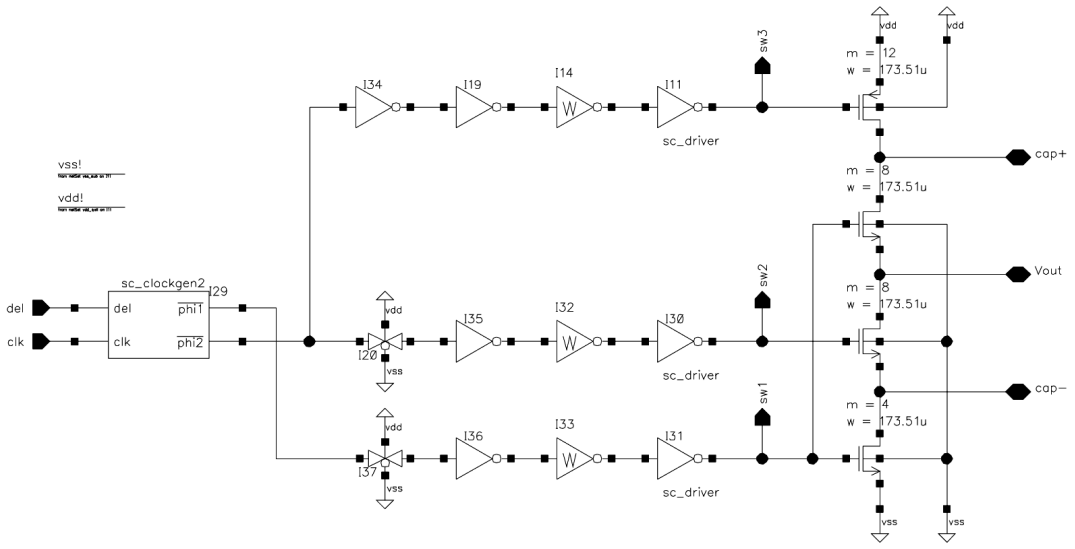

Figure 18: Circuit diagram for an implementation of a 2:1 voltage divider. The capacitors and the clock generator are external. The non overlapping two phase clock generator is on the left, followed by the driver stages and the four transistor switches. The capacitors and the clock generator, not showed in this diagram, are external.

The main challenge to design a charge pump is to find the best size for the MOSFETs to be used as switches. Figure 19 shows the calculated on resistance R_{ON} as a function of the operating point for an NFET and a PFET with 1 mm gate width. For a charge pump R_{ON} should be as small as possible at minimal transistor size. For this reason, NFET are generally preferred, because of their lower R_{ON}. Nevertheless, switches used at voltages close to Vdd are more practically integrated as PFETs, since in this configuration NFET transistors can not be driven correctly. In our implementation, we used a PFET for the top most switch (see Figure 18) and NFETs for the rest. The ratio of the size (gate width) of the transistors is chosen such that all transistors have approximately the same R_{ON}. The design can be scaled in size to optimize the efficiency for any specific load current. Since our target application is to power the frontend read out chip for the CMS pixel detector, we have optimized our design for the load current of this circuit, namely 24 mA. We found for the total size of the four transistor switches an area of 10,000 μm^2. In an optimized design, this area is proportional to the load current.

To calculate the efficiency of a charge pump we consider the equivalent circuit shown in Figure 20, where the circuit is represented by a perfect (lossless) voltage converter and two resistors representing the two power loss mechanisms.

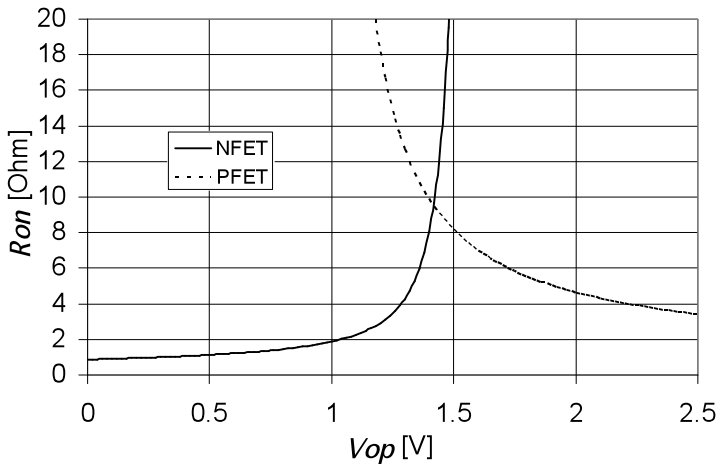

Figure 19: Calculation of the on resistance R_{ON} of a normalized NFET/PFET switch vs. operating voltage Vop = VD = VS. The supply voltage is 2.5V and the gate width is 1mm. R_{ON} scales with the transistor gate width.

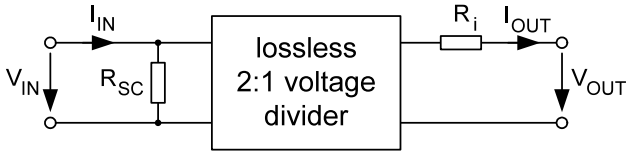

Figure 20: Equivalent circuit of the charge pump with the resistors representing the power losses.

The current through R_{SC} represents the current needed to drive the gate capacitances of the transistor switches. The power dissipation in this resistor is proportional to the frequency and to the square of the input voltage. This value is scalable and can therefore be adapted to any output load current.

Another source of losses is the power dissipation at the source resistance R_i. At this resistor we have a voltage drop (power loss) proportional to the output current. The value of this resistor depends on the frequency, the capacitor values and the on resistance of the transistor switches. To model R_i a formula has been derived for our circuit from the theory of switched capacitors filters. Figure 21 shows the result of the calculation for our present design. We have three main regions for R_i. For low frequencies, R_i is inversely proportional to the frequency. For high frequencies the limited switching time increases R_i with the frequency. For charge pumps we have to go for lowest possible R_i. For this reason the range of the switching frequency is limited between 1 and 20 MHz with 100nF capacitors. The value of R_i in this region is two times the on resistance R_{ON} of a transistor switch.

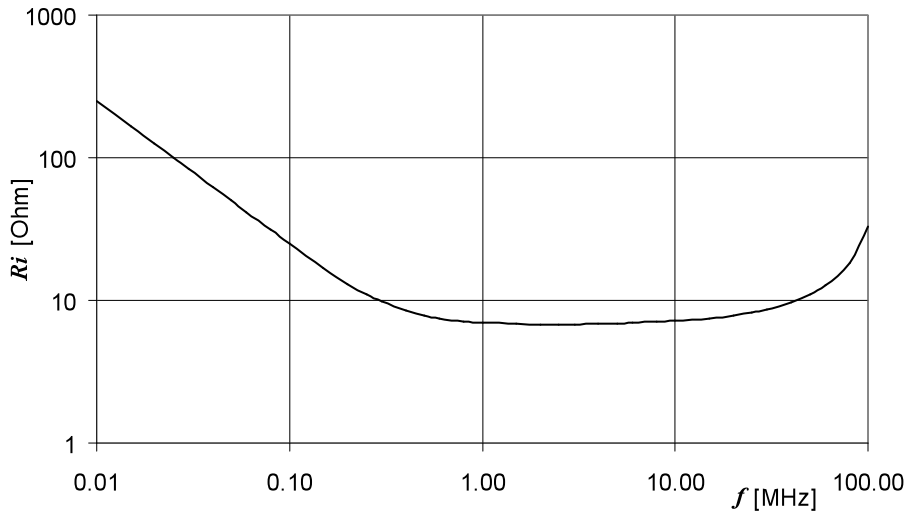

Figure 21: Calculated output resistance as a function of the switching frequency f for C = 100nF, R_{ON} = 3.3 Ohm. The flat region with the lowest R_i is the optimal operating frequency range.

8. CONCLUSIONS

The scheduled objective for the first year of activity of this work package was the evaluation of different conversion technologies for distributing power in SLHC trackers. As reported in this document, this task has been accomplished and as a result a power distribution scheme using two conversion stages has been proposed: a first conversion stage, implemented by a buck converter with air-core inductor, powering a full module is followed by an on-chip switched capacitor voltage divider.

In addition, progress has been made in view of the integration of the converters in the full detector system. This was possible with the development of dedicated methodologies and tools, including the use of sophisticated software for 3-D simulations of air-core inductors, the development and construction of reference measurement stations for conducted noise, the procurement and exploitation of available detector modules/systems of the LHC generation. Such tools and methodologies will be very valuable to guide the development and integration of a final stage-one converter (powering a full module and based on an ASIC), whose development is the main focus of the next year of activity of the project.