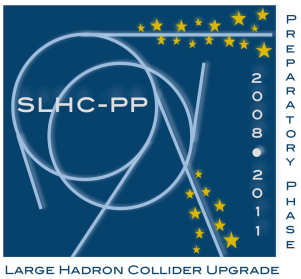

SLHC-PP

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The Preparatory Phase of the Large Hadron Collider upgrade (SLHC-PP) is a project co-funded by the European Commission in its 7th Framework Programme under the Grant Agreement n° 212114. SLHC-PP began in April 2008 and will run for 3 years.

TABLE OF CONTENTS

1. EXECUTIVE SUMMARY

Distribution of power to the electronics of the SLHC tracking detectors is a most challenging task. The number of channels of the SLHC tracking detectors is expected to increase by a factor of five to ten and, consequently, current consumption will increase by almost an order of magnitude compared with the LHC. New powering approaches must be identified, investigated and engineered to make tracking at SLHC possible.

Serial powering is one of the two main powering techniques studied in SLHC-PP Work Package WP8. Serial powering R&D has made very significant progress in the last year. The project targets of the first year of the SLHC-PP project have been fully reached and in many instances surpassed.

A number of serial powering systems, based on shunt regulators built from commercial components, have been prototyped. The systems (SCT modules and silicon strip supermodules) were characterized in detail and their system parameters investigated. We were able to demonstrate that serial powering systems can be operated with good electrical performance, using a minimum number of clock and control lines and with a single high-voltage line to bias several silicon sensors. The grounding and shielding scheme implemented in the supermodule prototypes proved to be effective.

We have specified and started developing custom serial powering regulators for both silicon pixel and strip detectors. These are early prototypes. They will enable us to build and characterize more sophisticated serial powering systems than was possible with commercial regulators and to gain crucial design experience for the final power electronics.

Finally, we have made significant progress on the specifications of protection systems, prototyped several schemes and are moving on to design a custom protection and bypass circuit.

2. INTRODUCTION

Serial powering is a novel and highly promising concept for power distribution in silicon particle detectors. With serial powering the power for the read-out electronics of detector modules is not provided independently or in parallel. Instead a constant current is run in series through shunt regulators placed on each module; the shunt regulators set the required module voltage levels. In serial powering current is “re-cycled” and the current required by a string of modules is identical to the current of a single module (see Figure 2.1). The total current distributed to a detector system can thus be reduced by large factors depending on the number of modules in series. The total voltage across the string of modules, on the other hand, is increased and each module in the string operates at a different potential.

The latter feature makes serial powering somewhat unorthodox and despite its significant benefits serial powering has not yet been implemented in a running particle physics experiment. The R&D on serial powering in SLHC-PP aims to provide the necessary tools, custom electronics and understanding to enable implementation of serial powering for silicon tracking at the SLHC.

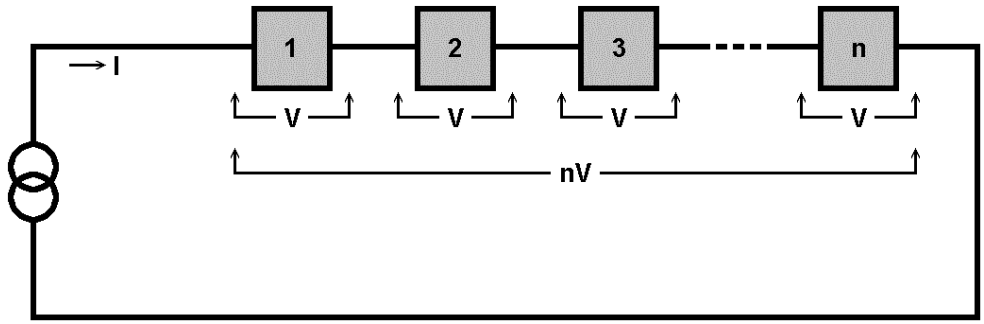

Figure 2.1: *Serial powering concept showing a constant-current source and n modules powered in series. The shunt regulators on each module are not shown.*

The first phase of the project, covered in this report, focuses on "generic studies" of serial powering. We wanted to gain operational experience with serial powering systems for silicon detectors in general, characterize the electrical performance of these systems and learn about practical difficulties and possible limitations. These "generic studies" have been very successful and are described in section 3. They are largely based on commercial serial powering components, since custom designs were not available for silicon strip sensors at the start of this project. A complete evaluation of serial powering relies on custom radiation-hard electronics, the design of which has started and provided first prototypes (see section 4). The development of the final power electronics will require significantly more effort and time and will be the focus of the second phase of the project.

Finally, we have started to develop a dedicated protection system to build extremely reliable serial powering systems. The status of this activity is covered in section 5.

3. GENERIC STUDIES WITH SERIALLY POWERED STAVES

The first system tests of serial powering with silicon strip sensors were performed using spare ATLAS SemiConductor Tracker (SCT) modules. For these and subsequent tests, the shunt regulators were built up with commercial electronics. The shunt regulator schematic is shown in Figure 3.1. A commercial power supply in over-current protection mode served as the constant-current source. The shunt regulator provides digital voltage to the ABCD readout integrated circuits (ROIC) of the SCT modules. Further circuitry (not shown in Figure 3.1) was built to provide analog voltage (using a linear regulator powered by the digital voltage) and for the AC-coupling of data, control and clock signals.

To test serial powering in a more integrated and compact arrangement as anticipated for the SLHC trackers, we built and characterized several silicon strip supermodules or staves. A 6-module stave and a 30-module stave were constructed[1]. Photographs of these objects are shown in Figures 3.2 and 3.3.

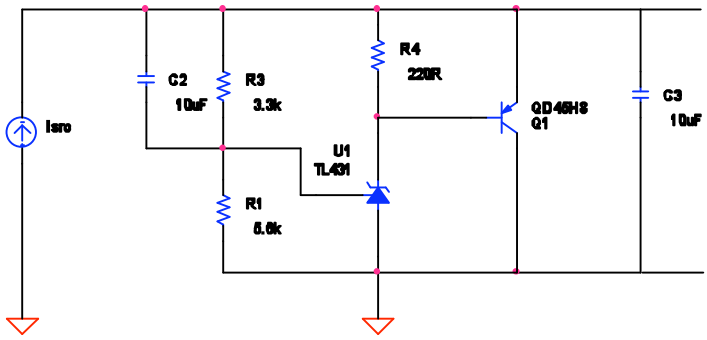

Figure 3.1: *Schematic of the shunt regulator circuitry with component names and values.*

Both staves are read-out using ABCD chips. The serial powering circuitry of the 6-module stave and the 30-module stave are identical.

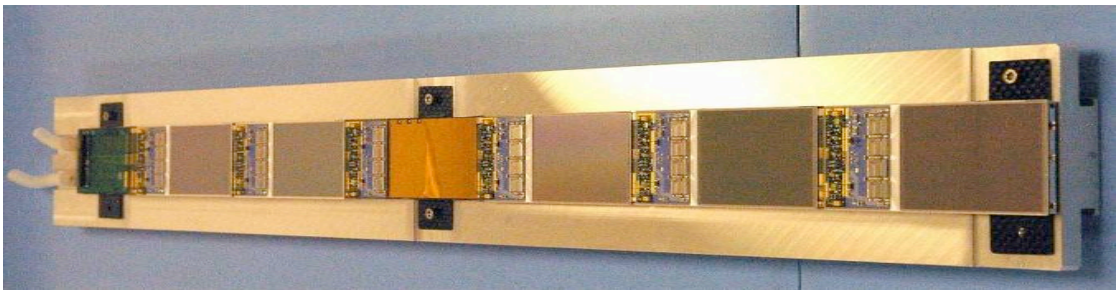

Figure 3.2: *Photograph of a 6-module serially powered stave on a bonding fixture. Five sensors and their corresponding hybrids plus a single hybrid are mounted on the stave. The green PCBs contain the serial powering circuitry.*

We managed to obtain a wealth of results from the testing of the 6-module stave, which include:

- The noise performance of the modules (with and without sensors) powered in series is excellent and compatible with individually powered modules.
- The stave can be operated from a single high-voltage line biasing the sensors.
- The AC-coupling of the clock and command LVDS signals in a multi-drop configuration is working.
- The grounding and shielding features of the stave, in particular the single-point connection of the local shields to their corresponding hybrid ground, is effective.

[1] The 6-module stave shown was built at RAL, the 30-module stave at LBNL

- Serial powering circuitry is rather compact.

These observations have been confirmed by the tests on the 30-module stave (which currently is half completed) and the 30-hybrid stave test vehicle. The serial powering circuitry of the 30-module stave was implemented directly on the hybrid, rather than on a separate printed circuit board (PCB). The hybrid with six ABCD chips and the serial powering components is shown in Figure 3.3. The size of the serial powering circuitry shown in this picture will be reduced by a large factor with custom circuitry. The shunt and linear regulators may be absorbed in the ROICs, depending on the chosen architecture (see section 4) and the size of the AC-coupling capacitors will be reduced due to the smaller supply voltage of the future ROICs.

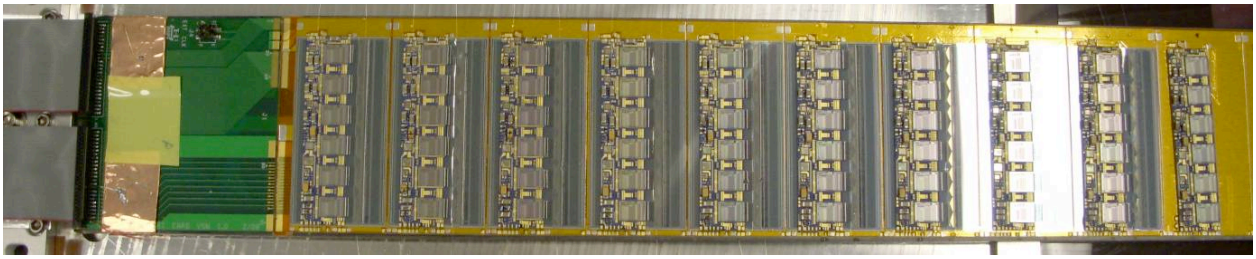

Figure 3.3: *Photograph of a partially assembled 30-module stave with serial powering.*

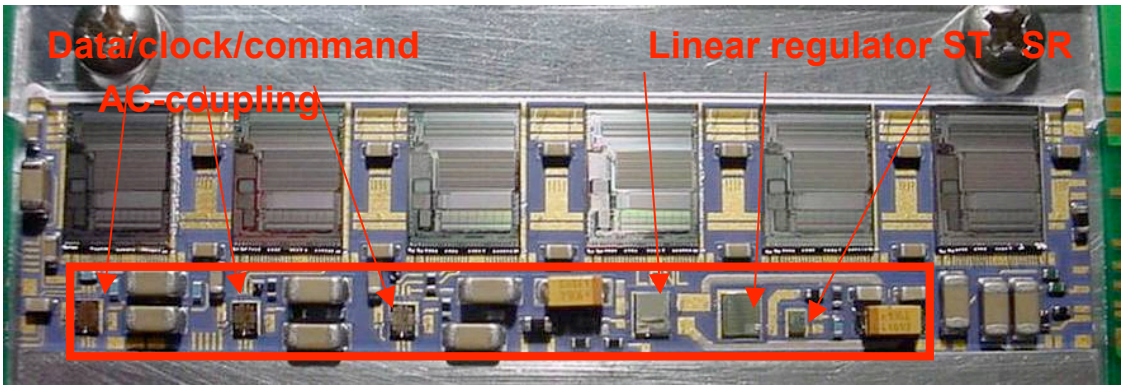

Figure 3.4: *The ceramic hybrid with six ABCD chips and RAL serial powering circuitry as used for the 30-module stave.*

Since the modules powered in series operate at a different potential, signals to and from the modules must be AC-coupled or optically de-coupled. Optical signal transmission on the stave does not seem practical at the SLHC and has thus not been investigated. Instead electrical signal transmission using DC unbalanced codes has found to be reliable at 40 MHz when the circuitry shown in Figure 3.5 is implemented. The circuitry can be further simplified if DC balanced codes are used, which is the current planning for ATLAS.

The experience gained with these prototypes enabled us to suggest a possible serial powering implementation for a 24-module silicon strip stave as shown in Figure 3.6.

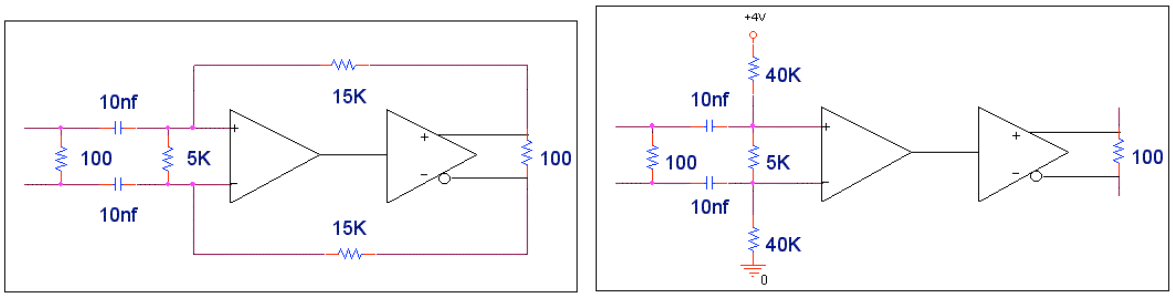

Figure 3.5: *Schematic of AC coupling circuitry (latch) suitable for multi-drop LVDS. (Left) DC unbalanced command signals. (Right) DC balanced clock signals.*

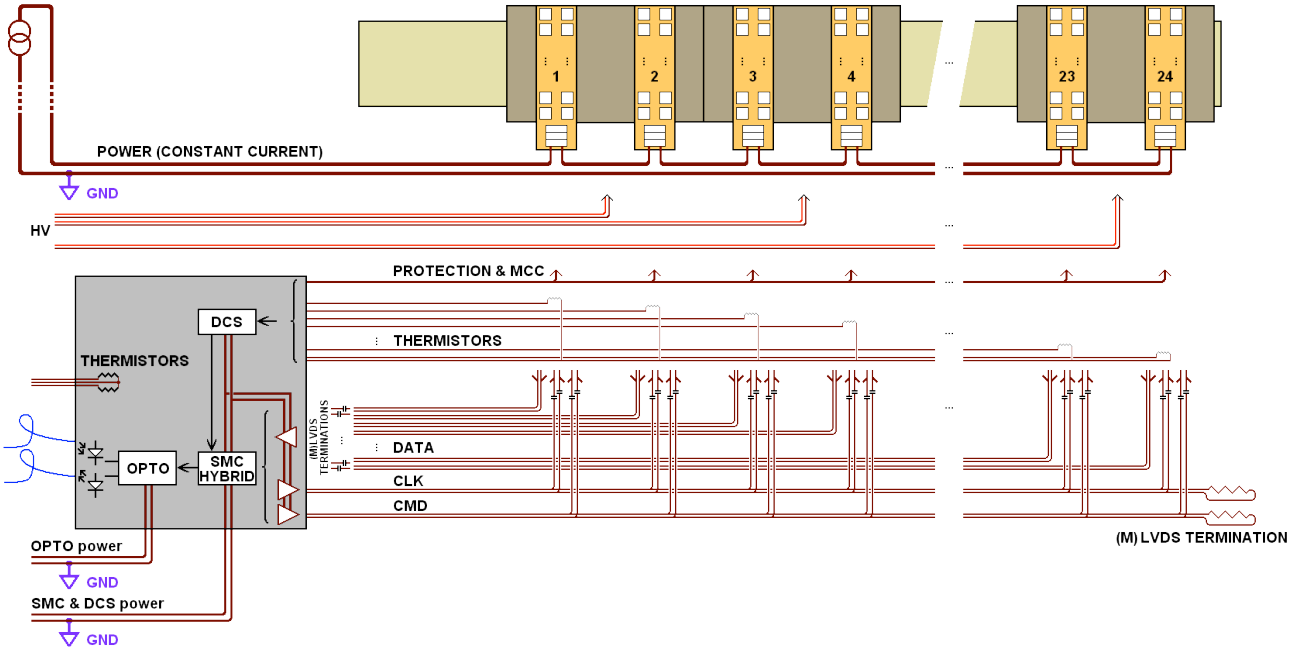

Figure 3.6: *Sketch of a possible implementation of serial powering for a short strip stave showing the protection, data, command, clock and high voltage lines. Only the top part of the stave is shown, the bottom part is electrically independent and identical to the top.*

4. SERIAL POWERING ARCHITECTURES, SPECIFICATIONS, AND FIRST POWER ELECTONICS PROTOTYPES

There are several conceivable serial powering architectures, which are shown in Figures 4.1 through 4.3. While each serial powering scheme will contain shunt regulators and shunt transistors, there are several plausible arrangements of these elements, which differ in the

number of regulators and transistors and their location. For the architecture of Figure 4.1, a single shunt regulator and transistor powers the module read-out chips (ROICs). For Figure 4.2, both shunt regulator and transistor are integrated into the ROICs and are connected in parallel. For Figure 4.3, a single or double shunt regulator drives several integrated shunt transistors.

Each architecture has its merits and without proper design and prototyping it is difficult to choose a favorite. We were able to design first ASIC prototypes to implement and investigate all three architectures.

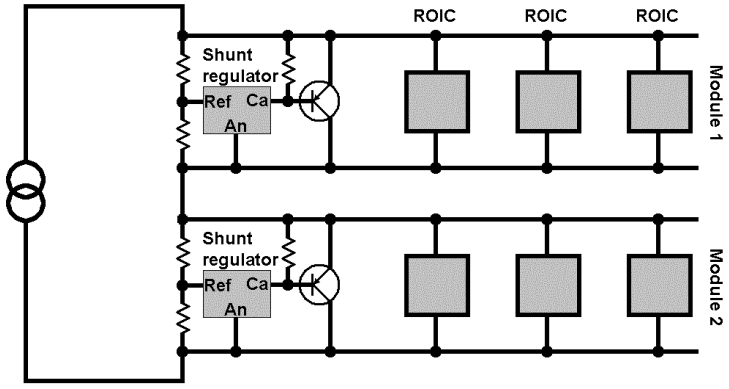

Figure 4.1: *A single shunt regulator and shunt transistor external to the ROICs.*

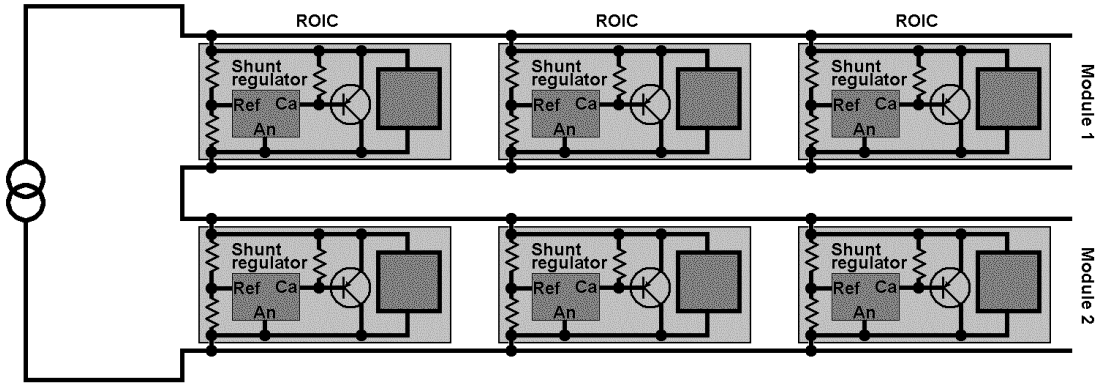

Figure 4.2: *Parallel shunt regulators and shunt transistors, one each in each ROIC.*

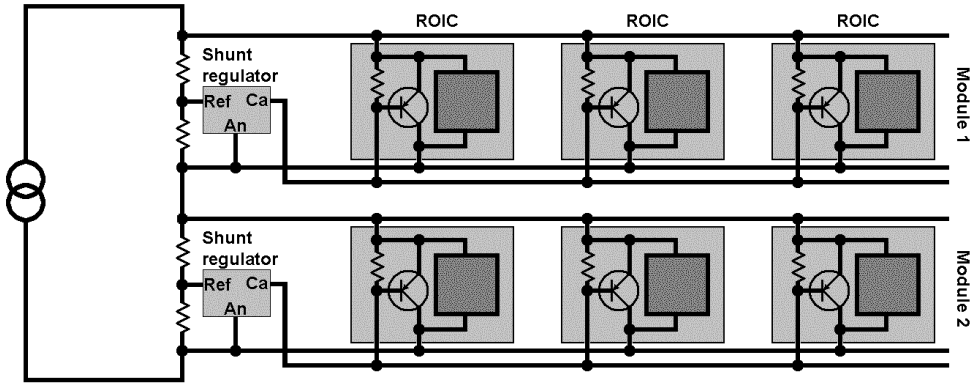

Figure 4.3: *A single external shunt regulator combined with parallel shunt transistors, one in each ROIC.*

One of the options of serial powering of silicon strip detector modules is a distributed system with the shunt regulators included in each ROIC (Figure 4.2). Such a system offers a number of advantages:

- power dissipated in the shunt regulators is distributed uniformly across the hybrid;
- no very high current devices are required;
- a critical single point-of-failure is eliminated, compared to solutions with one regulator per hybrid;
- the hybrid design can be fully scaleable with respect to power consumption.

In the distributed system the shunt regulators integrated in the readout ASICs must be connected in parallel on the module. A fundamental problem to be addressed and solved in such a system is its sensitivity to matching of parameters of individual shunt regulators. A novel shunt regulator circuit has been proposed and the prototype design has been integrated in the ABC-Next readout ASIC.

The conceptual schematic diagram of the developed shunt regulator suitable for connecting several shunt regulators in parallel on the hybrid is shown in Figure 4.4. In addition to the conventional shunt regulator, the design comprises circuitry responsible for limiting the current flowing through the shunt transistor at a preset level and adjusting the reference voltage and thus the output voltage of the regulator. The current of the shunt transistor is sensed and compared with six different reference currents. If the sensed current in one device exceeds the given reference current, the corresponding correction current source is connected to the input of the auxiliary transresistance amplifier. As a result the reference voltage for this shunt device is reduced and the current of the shunt device is limited. Since the output voltage of the shunt device under consideration increases by a few mV other shunt devices connected in parallel sink more current. It should be noted that this is a one-step operation and after which the correction current source remains connected while the feedback loop between the shunt transistor and the correction circuit is interrupted. This

solution ensures that the output impedance of the shunt regulator is not increased due to continuous operation of the correction circuit.

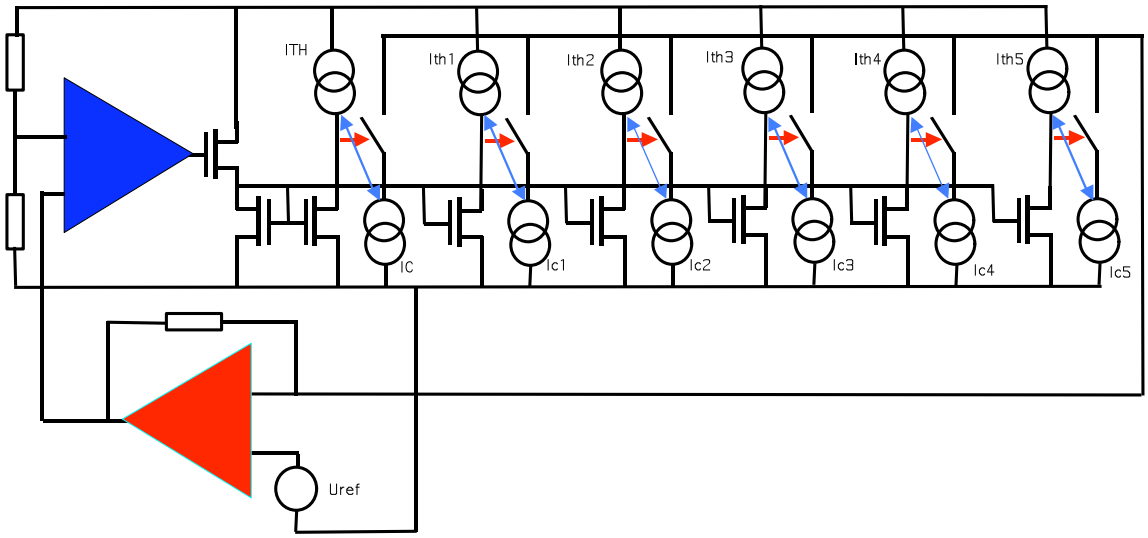

Figure 4.4: *Conceptual schematic diagram of the shunt regulator with auxiliary correction amplifier.*

The current threshold ITH in one of the six stages is set high, for the default configuration at 100 mA. This current is set by an internal resistor connected to the high supply voltage. The shunt regulator in the ABC-Next chip is equipped with two additional internal resistors connected to the bonding pads, which can be bonded to the high supply voltage in parallel with the one connected permanently. Selecting an appropriate combination of the internal resistors one can set the current threshold ITH at one of the following values: 100 mA, 150 mA, 200 mA, 250 mA. This stage works like an over-current protection circuit in cases when no digital switching current is drawn by the ABC-NEXT chip and the supply has to be taken by the shunt device. The other five stages work according to the same principle, but their role is to redistribute the current between shunt devices in normal steady-state operation so that the shunt currents and the output impedances of the shunt devices connected in parallel are of the same order of magnitude. The nominal current thresholds Ith1 to Ith5 in the five stages are scaled with the following ratios: 5: 4: 3: 2: 1. When the shunt current in the device exceeds a given threshold, the corresponding correction current is switched on and the reference voltage is adjusted accordingly.

The performance of the circuit has been simulated extensively considering various powering scenarios of the silicon strip detector modules powered serially. An example of operation of 20 shunt regulators connected in parallel is illustrated in Figure 4.5. The mismatch of device parameters is modelled by varying the reference voltage of each shunt regulator by ±10 mV around its nominal value. The plots show the transient waveforms of the output voltage and the currents in individual shunt devices for a supply current ramp-up time of 1 ms. One can see that the total current is distributed uniformly in all individual shunt devices. Using the conventional shunt regulator design instead, would result in the total current flowing through only one of the 20 devices.

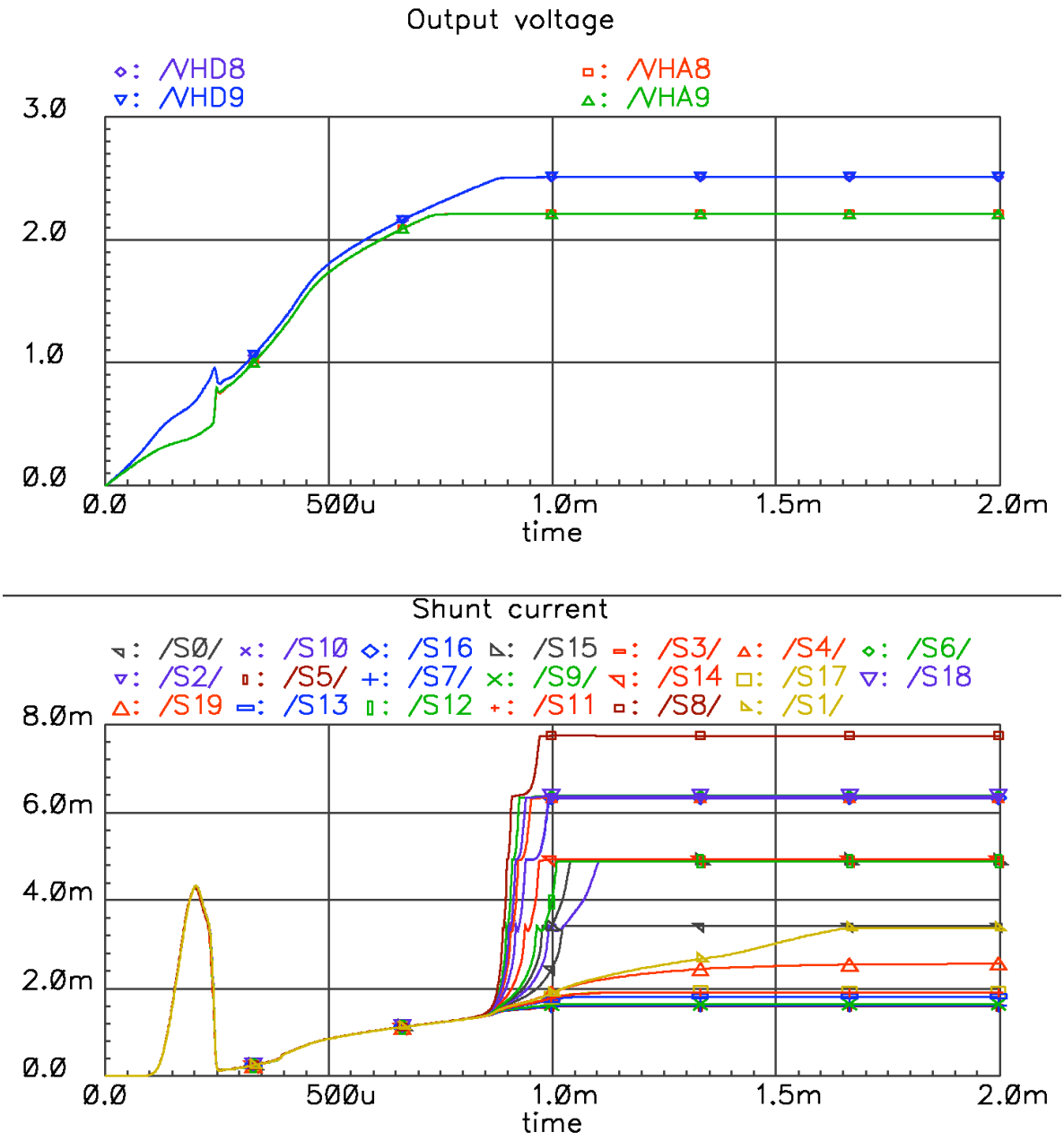

Figure 4.5: *Output voltages (upper plot) and shunt currents (lower plot) for 20 shunt regulators connected in parallel assuming a supply current ramp-up time of 1 ms.*

The design has been implemented in a 0.25 μm CMOS process and integrated in the power management circuitry of the ABC-NEXT readout chip. The layout of shunt regulator has been integrated together with the serial regulator in a single block of area 1.5×0.6 mm^2. The mask layout of the regulator block is shown in Figure 4.6.

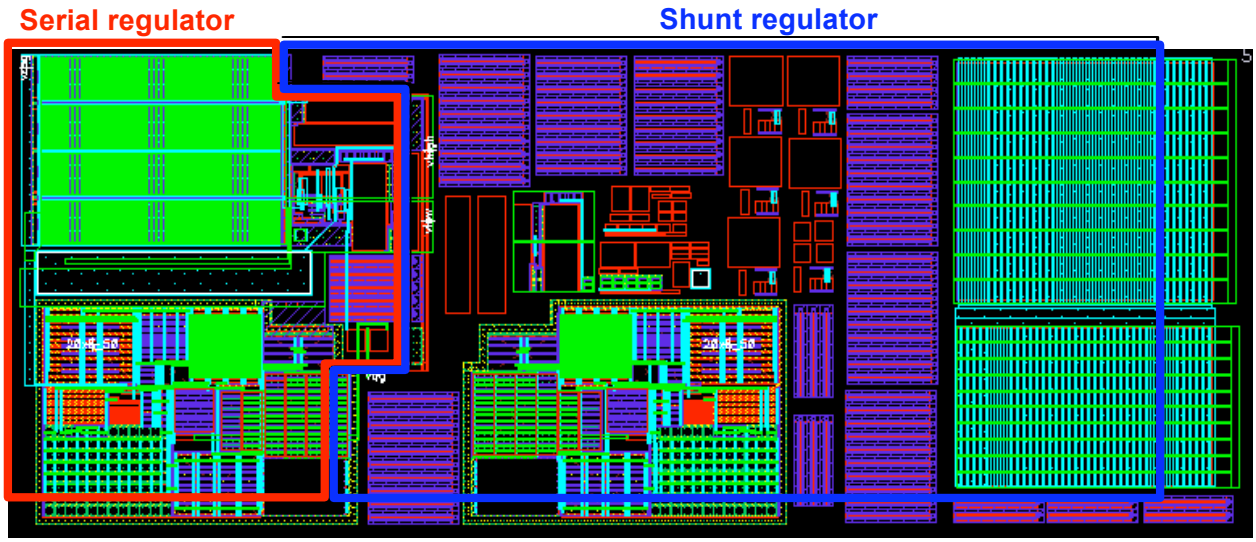

Figure 4.6: *Mask layout of the shunt regulator implemented in the ABC-NEXT design.*

The serial powering architectures shown in Figures 4.1 and 4.3 can be implemented using the SPi chip. SPi is a generic serial powering chip specified by RAL. It was designed by FNAL and Penn University in 0.25 µm CMOS technology.

The chip contains the main elements required for serial powering (see Figure 4.7). To realize the architecture shown in Figure 4.3, a SPi shunt regulator is used to drive the parallel shunt transistors implemented in the ABC-Next chips. SPi is currently being characterized and so far seems to be functional. SPi combined with the ABC-Next prototypes will enable us to study all SP architectures in detail for silicon strip detectors and to identify the most promising or practical implementation.

In the description above we have ignored the fact that two different voltages are required by most ROICs in particle physics instrumentation: analog and digital voltage. For the current ABC-Next iteration in 0.25 µm CMOS, digital voltage of 2.5 V is set by the shunt regulator while the 2.2 V analog voltage is provided by an additional regulator (one regulator per chip). Alternatively both the shunt regulator and the linear regulator could be external to the ROICs as shown in Figure 4.1. This scheme could be realized using SPi.

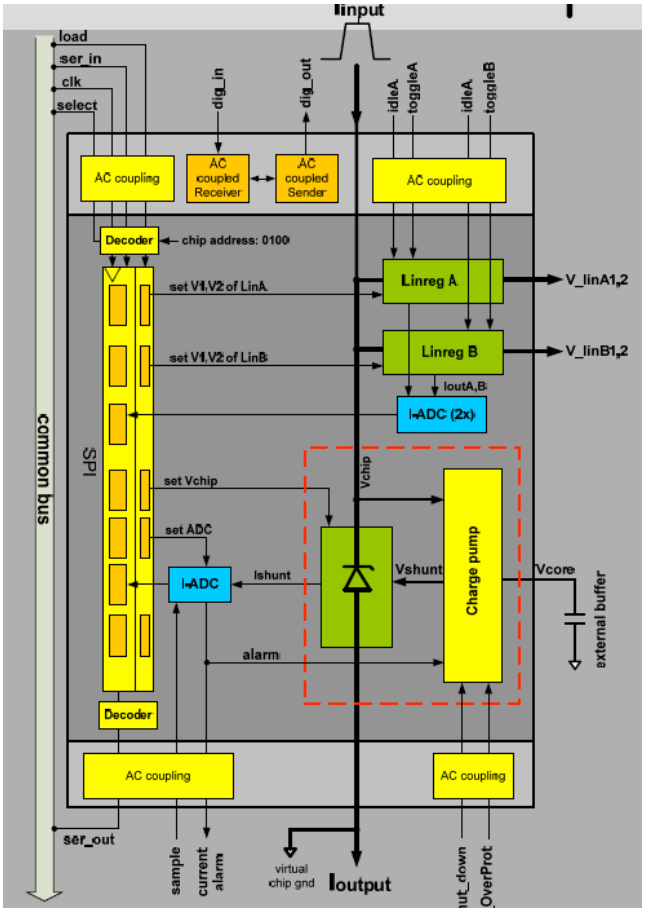

Figure 4.7: *A block diagram of the SPi chip with shunt regulators shunt transistors, two linear regulators, LVDS comports and more.*

The above arrangement is natural if digital voltage is larger than analog voltage. For future versions of readout chips in 130 nm CMOS, digital voltage will, however, be lower than analog voltage. We expect 0.9 V digital and 1.2 V analog voltage. Then other schemes to derive both voltages are required, some of which are shown in Figure 4.5. Some of the schemes above make use of integrated DC-DC converters. The R&D on integrated DC-DC

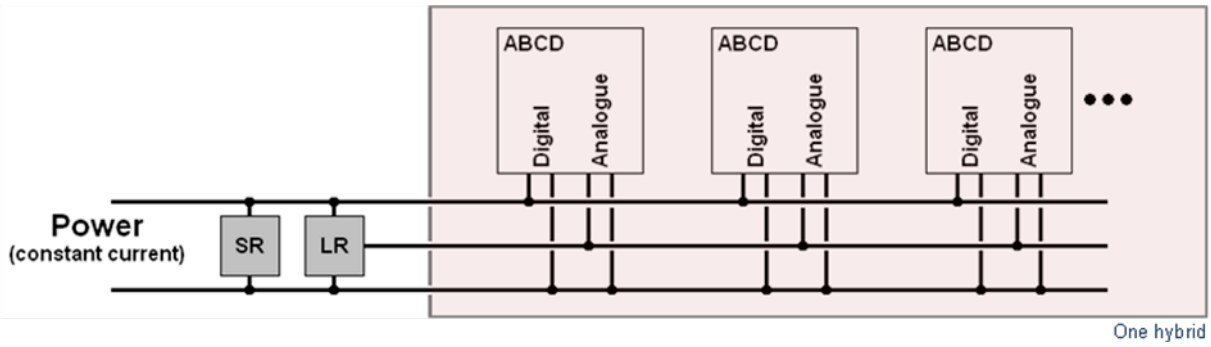

Figure 4.4: *A single shunt regulator and shunt transistor external to the ROICs.*

converters is an independent R&D topic of SLHC-PP Work package 8. The current status of this R&D is covered elsewhere.

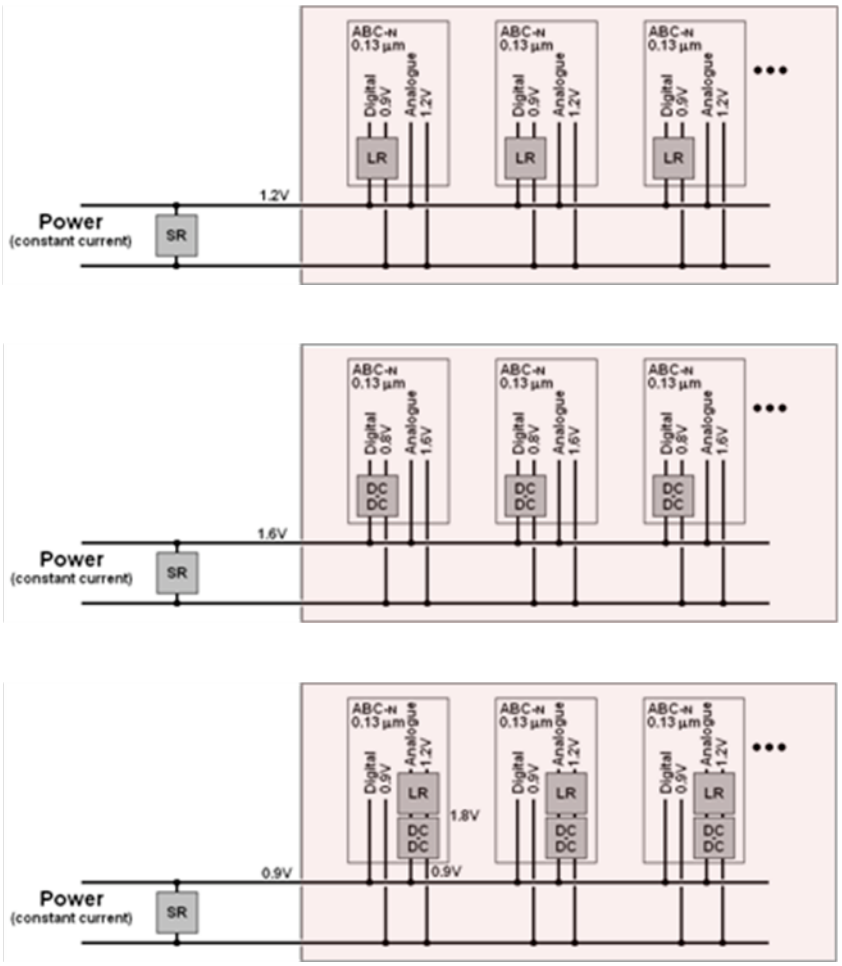

Figure 4.5: *A single shunt regulator and shunt transistor external to the ROICs.*

For serial powering of pixel modules an alternative to the schemes of Figure 4.5 is investigated in which all voltages are generated within the ROIC of the module without using DC-DC converters. Because up to four ROICs make up one module, the necessary shunt regulators have to be connected in parallel. To generate the required second, lower input voltage an LDO (or DC-DC converter) could be used. For simplification of this scheme and improvement of the failsafe behaviour a new shunt regulator circuit has been designed which allows an easy implementation of current balancing between regulators connected in parallel on one module and features different output voltages at the same chip. Two identical Shunt-LDOs (Shuldo) connected in parallel to the constant current input can therefore generate both needed supply voltages of the ROIC independently from the required voltage settings.

A key feature of the circuit is the integration of the shunt as a regulated resistor at the output of the LDO enforcing a constant current flow over the regulator. This is achieved with a

current comparison to a defined adjustable reference keeping the current over the shunt constant; see Figure 4.6 (left). To allow testing of different powering schemes, the same circuit can also be used as standard LDO by simply setting the reference current to zero. Two Shuldos will be implemented into the next ROIC generation (FE-I4) of the ATLAS pixel project enabling all necessary testing of serial powering schemes.

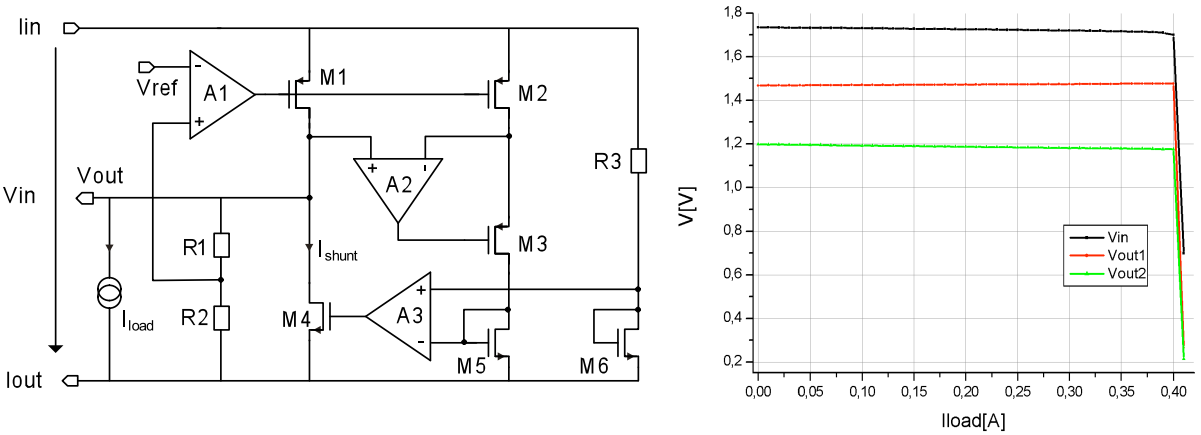

Figure 4.6: *(Left) Simplified schematics of the* Shuldo*. (Right) Measured output voltages of two Shuldos at different voltage setting connected in parallel vs. I_{load} of the lower channel. I_{load} of the higher output channel is fixed to 400mA.*

A first test chip with this circuit has been submitted in 130nm technology in September 2008 and tested successfully after fabrication. Figure 4.6 (right) shows the output characteristics of two regulators connected in parallel at different output voltages. The stability is excellent und agrees with the simulated performance. The effective output impedance including the wire-bonds and PCB traces needed for testing is about 50-60 mΩ. A small problem with the distribution of the currents between the regulators has been identified and will be fixed for the next iteration and the final implementation into the pixel ROIC, the FE-I4.

5. PROTECTION AND STAND-BY SCHEMES

There are several potential failure modes in a SP system, which could lead to the loss of the complete chain of modules. These are illustrated in Figure 5.1. One concern, sketched at the bottom of Figure 5.1, would be the injection of noise along the power line due to a mal-functioning module. This scenario has been studied in great detail using artificial noise sources and has been found not to be critical.

The most relevant single-point failure seems to be the interruption of the current flow through the modules due to a broken connection, e.g. a broken wire bond. Solidly engineered connections and/or a redundant serial powering trace would be important to minimize the failure probability. Another very effective protection against this failure is shown in Figure 5.2.

A dedicated bypass circuit (switch) can be enabled to provide an alternate current path if the connection to/through the module becomes faulty.

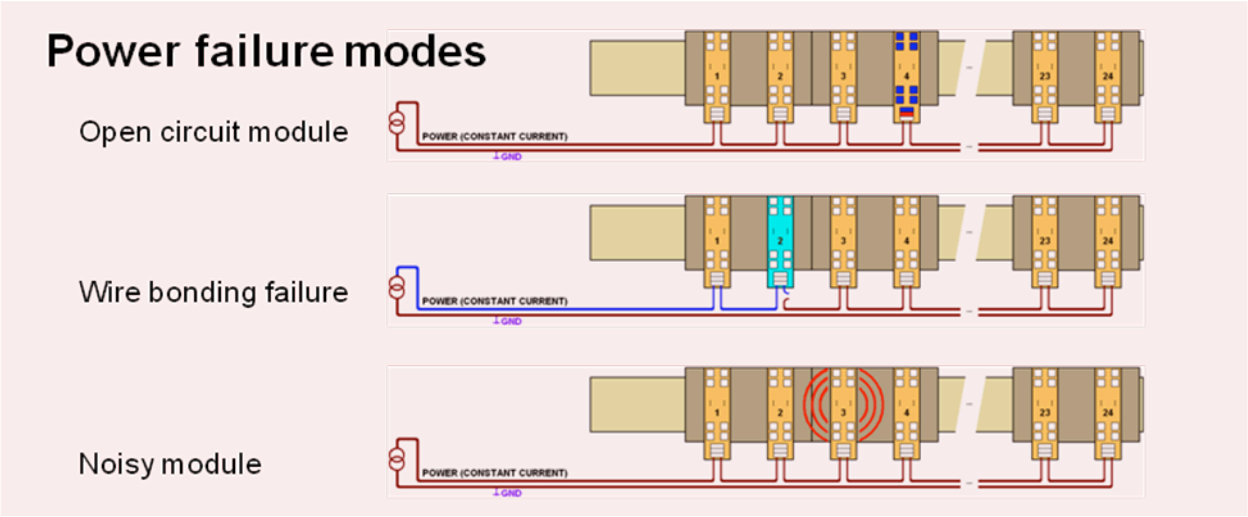

Figure 5.1: *Illustration of possible failure modes for serial powering of a silicon supermodule. (Top) One, several or all readout chips lose the power connection to the module. (Middle) A wire-bond or other connection from the power cable to the MCM is interrupted. (Bottom) A module becomes noisy and interferes with the other modules along the power line.*

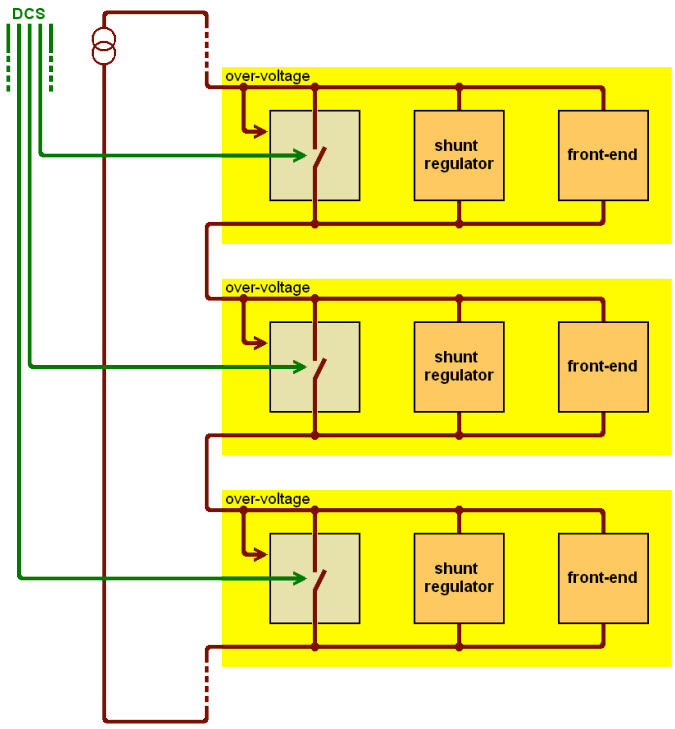

Figure 5.2: *Protection scheme of a serially powered chain of pixel modules. Each module has an independent protection control line (DCS).*

Each module carries its own bypass and protection chip, which allows us to disable a given module from the chain via a control line enabling an on-chip bypass transistor. A real-time overvoltage protection is implemented by a silicon controlled rectifier (SCR) which may enable the same bypass transistor independent from the control line. For simplicity each module bypass circuit is addressed directly with an extra AC coupled wire coming from the DCS system. While this introduces more material into the system the extra lines can be used to monitor the module voltages independently.

The schematics of the bypass circuit are shown in Figure 5.3. The key component is a MOSFET bypass transistor capable of shunting the full current of the SP chain of up to 3.5 A. The control signal will be an AC signal with a certain frequency provided by the DCS system. The overvoltage protection trigger threshold will be adjustable in a range between 1.4 and 1.8 V. The chip itself will be designed in 130 nm CMOS technology. Special care will be given to the radiation tolerance since the bypass chip has to withstand the same radiation load as the pixel modules. The specification of the Module Protection Chip (MPC) has been defined and chip design has already been started.

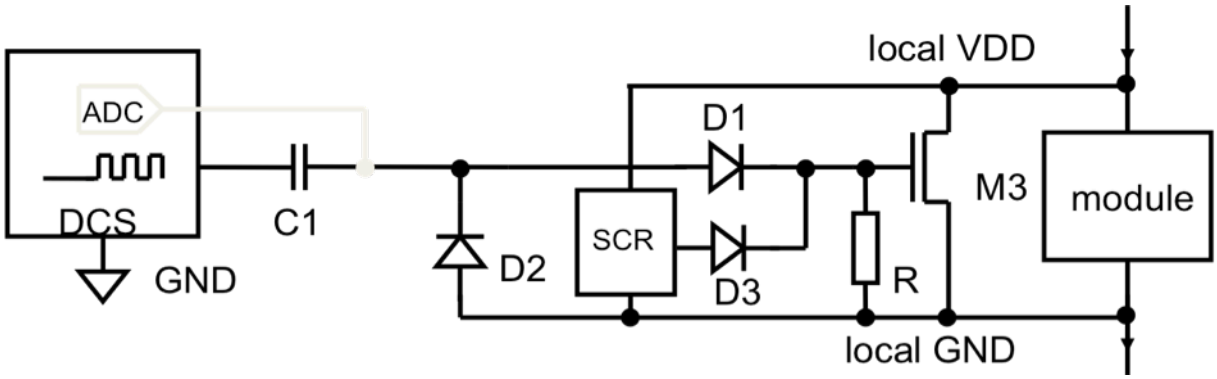

Figure 5.3: *Basic scheme of the module protection chip (MPC).*

A larger number of modules will be put in series for silicon strips than for pixels. For silicon strip modules, a single protection control line may thus be more natural to save material. This can be implemented using a “one-wire” type control scheme. There are different ways to control the bypass transistor. An alternative to the scheme in Figure 5.3 is shown in Figure 5.4. Here a small DC voltage common to all modules is used to drive an oscillator, which produces an AC voltage. The AC voltage is rectified, multiplied and referenced to module ground. It can be used to switch the bypass transistor and power other elements of protection and monitoring logic. The schematic shown has been simulated and prototyped and works as expected.

Finally it should be noted that some protection and monitor circuitry has also been implemented into the SPi chip.

We will continue prototyping and testing serial powering protection circuitry with the next version of serial powering supermodule prototypes.

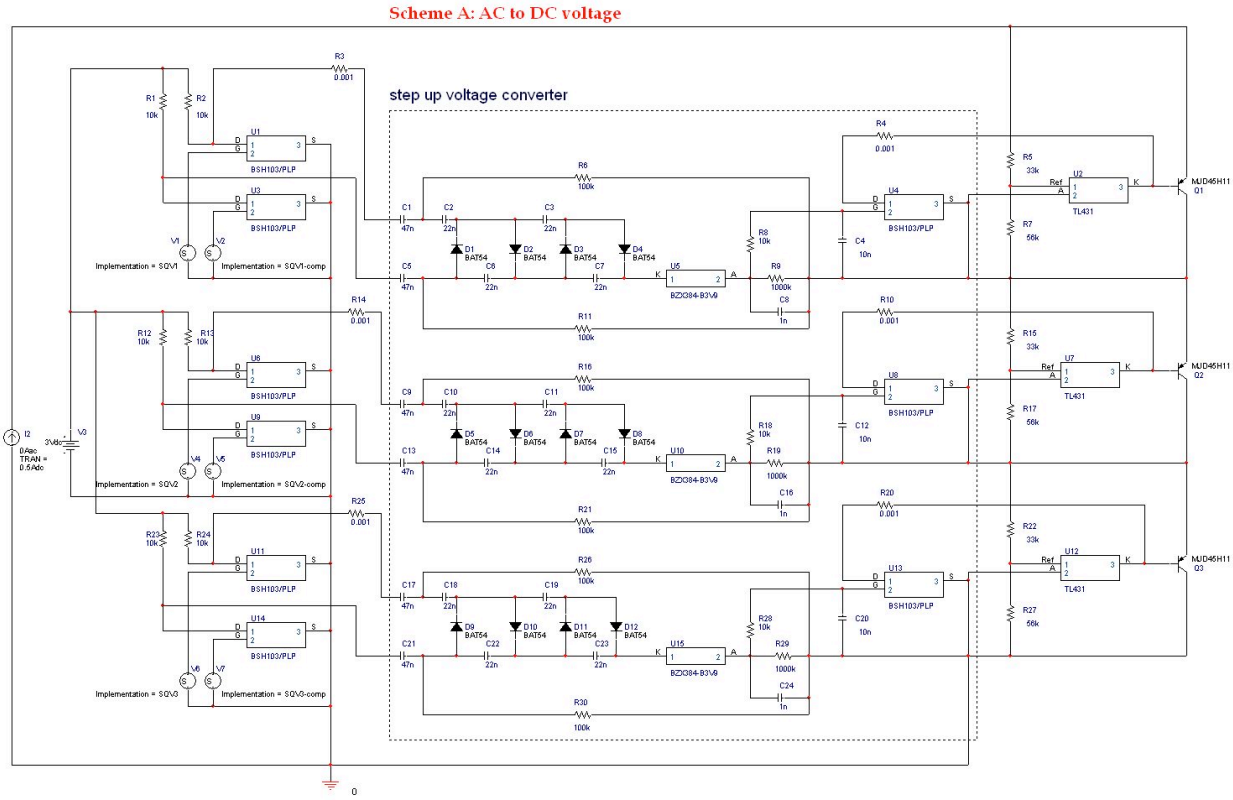

Figure 5.4: *Illustration of the RAL protection scheme for three modules in series. The one-wire system and the real-time overvoltage protection elements are not shown.*

6. CONCLUSIONS

The R&D effort on serial powering described in this document has been very successful. The system properties of serially powered supermodules are much better understood than one year ago and so far no show-stoppers could be identified. A number of independent serial powering systems have been assembled and significant operational experience has been gained. The noise performance of these systems is very satisfactory. The AC coupling of LVDS control and clock signals in a multi-drop configuration has been demonstrated. The chosen grounding and shielding scheme is effective.

The silicon strip SP systems operated so far are based on shunt regulators built from commercial components. While these are entirely adequate to investigate generic system properties, the final electronics must be radiation-hard custom designs. Different architectures to implement serial powering on a silicon detector multi-chip module have been identified. The corresponding circuitry has been specified and designed. First prototypes are available in 0.25 µm CMOS technology and are being characterized. The experience gained in this step will be crucial for the design of future prototypes in the final ASIC technology (which is likely to be 130 nm or 90 nm CMOS). These powering ASICS will also be used to build better and more realistic serially powered supermodules.

Protection schemes to prevent single-point failures and the loss of several modules have been identified and are being prototyped. The first results are promising.