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The Preparatory Phase of the Large Hadron Collider upgrade (SLHC-PP) is a project co-funded by the European Commission in its 7th Framework Programme under the Grant Agreement n° 212114. SLHC-PP began in April 2008 and will run for 3 years.

TABLE OF CONTENTS

1. EXECUTIVE SUMMARY

Two schemes of serial powering of detector modules for SLHC trackers are being developed: for the pixel detectors and for the silicon strip detectors. Custom-designed ASICs comprising shunt regulators and linear regulators have been developed for each of the detector systems. The project targets defined by deliverable 8.2.2 have been fully reached.

The three different designs of the shunt regulators, which can be used as building blocks for serial powering systems, include:

- Shunt-LDO regulator for serial powering of pixel modules. In order to provide the pixel modules with the needed supply voltages of 1.2 V (analog) and 1.5 V (digital) a new on-chip power regulator has been developed, which combines the functionality of a shunt regulator with that of a low-dropout (LDO) voltage regulator. It is planned to equip each pixel front-end chip (FE-I4) with two of them. Redundancy is achieved by using eight regulators in a pixel module consisting of four chips. A first test chip with this circuit has been submitted in radiation-hard 130 nm technology in September 2008, tested successfully after fabrication. Preliminary results were shown in the previous report. The chip worked according to the specifications. The distribution of shunt currents among the regulators was found to be unequal during the ramp-up phase, starting at an input current of ~300 mA. The problem was identified and corrected. A second test chip has been submitted in March 2009 and the test results have shown that the problem was understood and solved correctly.
- Shunt regulators in the ABCN-25 readout ASIC. The ABCN-25 ASIC for readout of silicon strips comprises two prototypes of distributed shunt regulator circuits, which can be used alternatively. One circuit is a full shunt regulator. Another circuit comprises only shunt transistors, with gate control inputs, which are foreseen to be driven by an external voltage control loop, common for all ASICs connected in parallel on the hybrid. Each of the two designs, which can be used alternatively, allows connecting several shunt regulators in parallel on the hybrid. The circuits have been tested and parameterised using dedicated evaluation boards. The test results show that both circuits are fully functional according to the specification. Further, the serial powering modes have been demonstrated to work correctly for the fully populated hybrids comprising twenty ABCN-25 ASICs, which means twenty shunt regulators connected in parallel.
- SPi ASIC for serial powering strip detector modules. The SPi (Serial Powering Interface) is a versatile chip including a shunt regulator and other circuitry, like AC-coupled interfaces and protection circuits, needed in the serially powered system. The chip has been fully tested using a dedicated evaluation board and. The measured performance show that the chip can be used for on the considered option for serial powering of silicon strip detector modules, i.e. with a single shunt regulator per hybrid comprising twenty ABCN-25 readout ASICs.

2. INTRODUCTION

Design studies summarized in report SLHC-PP-8.2.1-982423-v1.4 have shown that the serial powering is a promising and feasible solution to provide power to the pixel detector modules and strip detector modules in the SLHC tracking detectors. Implementation of the serial powering schemes requires development of custom-designed ASICs (Application Specific

Integrated Circuits in the same radiation hard technologies, which are used for the readout ASICs. In the frame of the SLHC-PP project three types of custom regulators have been developed: (1) Shunt-LDO regulator for the serial powering of pixel detector modules, (2) shunt regulator implemented in the readout ASIC for silicon strip detector modules, which becomes a part of the distributed shunt regulator system in up to twenty readout ASICs used for reading out one hybrid, (3) high current shunt regulator, which is used to control the common supply voltage for all readout ASICs on the hybrid.

In this report we present a comprehensive overview of the design concepts and test results obtained for the prototype ASICs.

3. SHUNT-LDO REGULATOR FOR THE PIXEL DETECTOR POWERING SYSTEM

In order to provide the pixel modules with the needed supply voltages of 1.2 V (analog) and 1.5 V (digital) a new on-chip power regulator has been developed, which combines the functionality of a shunt regulator with that of a low-dropout (LDO) voltage regulator. It is planned to equip each pixel front-end chip (FE-I4) with two such regulator circuits. Redundancy is achieved by using eight regulators in a pixel module consisting of four chips.

A first test chip with this circuit has been submitted in radiation-hard 130 nm technology in September 2008, tested successfully after fabrication. Preliminary results were shown in the previous report. The chip worked within the specifications. The distribution of shunt currents among the regulators was found to be unequal during the ramp-up phase, starting at an input current of ~300mA. The problem was identified as due to a bad mirroring accuracy for non-saturated transistors. A second test chip has been submitted in March 2009.

3.1. FUNCTIONAL PRINCIPLE AND DESIGN OF THE SHUNT-LDO REGULATOR

The principle of the Shunt-LDO regulator is realized by the circuit shown in Fig. 1. The LDO regulator is formed by the error amplifier A1, the PMOS power transistor M1 and the resistive divider formed by the resistors R1 and R2. The supply current is flowing into transistor M1 and the transistor M1 is steered to create a voltage drop *VDS* between regulator input Iin and the output voltage terminal Vout such that the wanted output voltage is generated with respect to the current output terminal Iout, which corresponds to the local ground potential. The shunt transistor M4 is added to this LDO scheme to provide an additional current path to the regulator output Iout. To sense the amount of current that is flowing through the regulator, a fraction of the current flowing through transistor M1, which is defined by the current mirror aspect ratio k formed by transistor M1 and M2, is drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor M3 are added to improve the mirroring accuracy. For an ideal amplifier without offset, the voltage difference between the drain of the transistor M1 and the drain of transistor M2 is zero. Thus the value of the copied current is not affected by the low output impedance high current transistors have in this technology, because transistor M1 and M2 see the same *Vgs* the same *Vds* voltage as well. A reference current that depends on the input potential *Vin* is defined by the resistor R3. This current is drained into the gate-drain connected transistor M6.

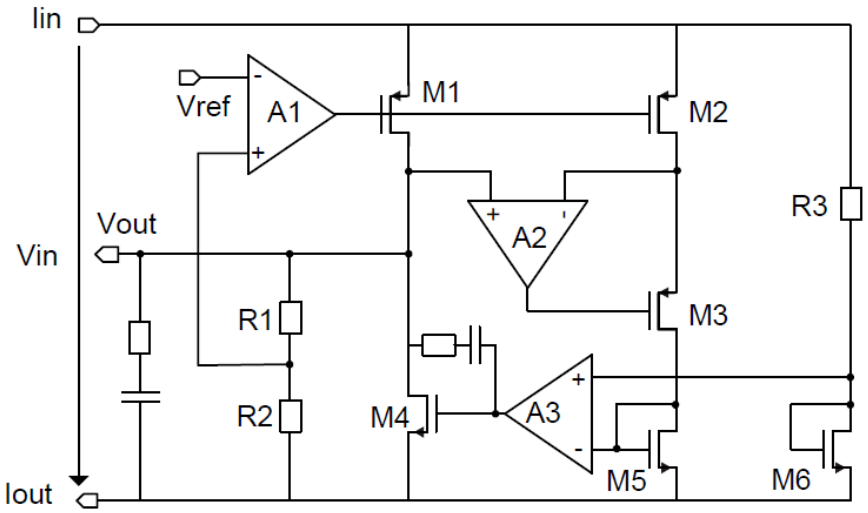

Fig. 1: LDO regulator with shunt capability (ShuLDO).

The reference current is compared to the fraction of current flowing through transistor M1 by use of the differential amplifier A3. If the current drained to transistor M4 is smaller than the reference current, the shunt transistor M5 is steered to draw more current and vice versa. By this means the current that is not drawn by the load is shunted through the transistor M5 and as a result a constant current is flowing through transistor M1. The regulator behaves like an ohmic resistor with respect to the voltage drop *Vin* across the regulator.

In the same way, a current would be split evenly between parallel placed resistors of same resistance, the shunt current will be distributed uniformly on parallel placed regulators. As a result, a robust parallel operation of Shunt-LDO regulators is possible with the proposed regulation scheme. In addition, the output voltage that is generated by the regulator has no influence on the equivalent regulator input resistance. As a consequence, Shunt-LDO regulators generating different output voltages can be operated in parallel and supplied by the same input current source.

In Fig. 2, a simulation of the parallel operation of two regulators is shown, having an output voltage of 1.5 V and 1.2 V respectively. In the upper plot of Fig. 2, it is shown that the input potential *Vin* is rising linearly with increasing input current. The output voltages *Vout*1 and *Vout*2 follow the input potential *Vin* until the referenced voltage levels are reached. As can be seen in the lower plot of Fig. 2, the currents flowing through the regulators are exactly the same. In a real system, mismatch and process variation will lead to variation of the resistor R3 used as a reference of about 10-20% with an according influence on shunt current distribution. For stable operation of the Shunt-LDO regulator, two regulation loops have to be studied and compensated. One regulation loop is voltage based and corresponds to the LDO regulator part of the circuit. For this loop, the standard LDO regulator compensation strategy is applied. A dominant pole is introduced to the regulator output by use of an external capacitor. The Equivalent Series Resistance of the output capacitor introduces a zero which compensates the pole which is related to the error amplifier output impedance and the gate-source capacitance of the PMOS power transistor. The second regulation loop is current based and corresponds to the shunt circuitry. For this loop, a zero is introduced by an internal RC network which is connected between gate and drain of shunt transistor M4. Both loops have been designed to have a phase margin of minimum 65 degrees in the whole region of operation.

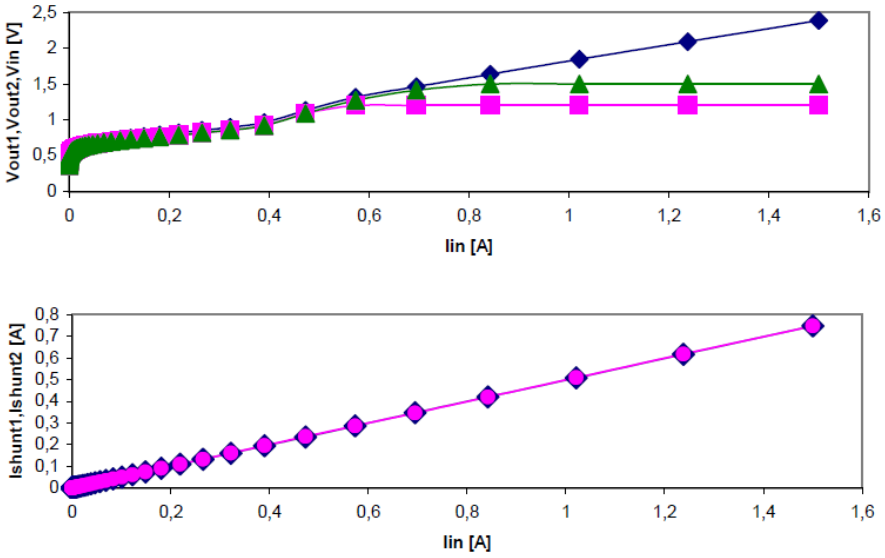

Fig. 2: Simulation result of parallel operation of two Shunt-LDO regulators.

A Shunt-LDO regulator prototype has been implemented and produced in a 130 nm CMOS technology. The mask layout is shown in Fig. 3. The prototype has been specified to generate voltages in the range of 1.2-1.5 V and to cope with a shunt current of up to 500 mA. The reference resistor R3 has been chosen to be 4 kΩ and the current mirror aspect ratio factor k has been set to 1000.

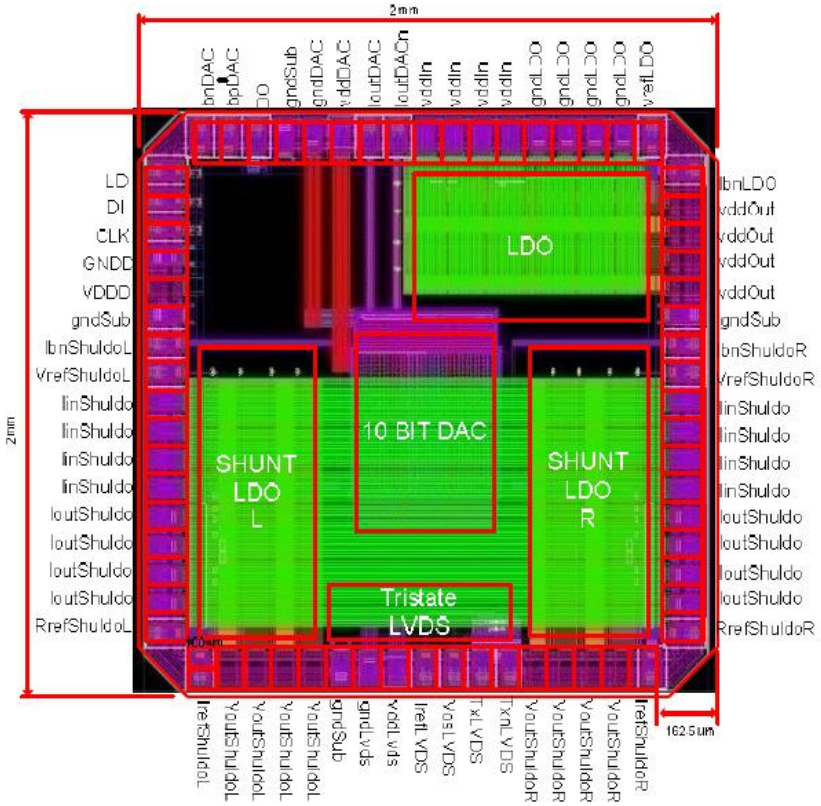

Fig. 3: Mask layout of the Shunt-LDO chip in 130 nm technology.

3.2. TEST RESULTS

The performance of the prototype Shunt-LDO ASIC has been evaluated using a dedicated test board with two Shunt-LDO regulators connected in parallel, shown in Fig. 4. Possibility of connecting the Shunt-LDO regulators in parallel is a unique feature of the developed circuitry.

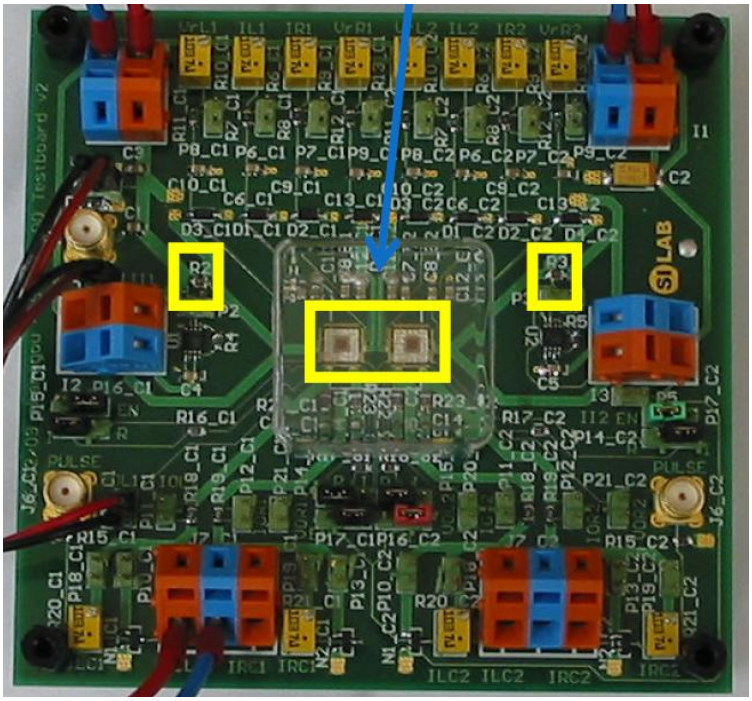

Fig. 4. Test board with two Shunt-LDO regulators connected in parallel.

In Fig. 5, the measured IV-voltage characteristic of two parallel placed regulators is shown, where one regulator is generating an output voltage of 1.2 V and the other an output voltage of 1.5 V. As has been predicted by the simulation, the voltage drop *Vin* across the regulator rises linearly with input current as soon as a voltage potential *Vin* is reached where all transistors in the regulator are saturated. The output voltages follow the input voltage potential *Vin* until the referenced output voltages are reached. The measured slope of *Vin* is equivalent to a 2 Ω resistor which corresponds to the input impedance of two parallel placed regulators.

In Fig. 6, the measured load regulation performance is depicted. A load current is drawn out of the regulator generating the output voltage of 1.2 V which causes a slope at the output voltage which corresponds to 60 mΩ including wire bond and PCB parasitics. Taking into account the length and the specific resistance of the used wire bonds, the effective output impedance of the regulator is measured to be less than 30 mΩ. The voltage output of the parallel operating regulator generating the 1.5 V stays unaffected.

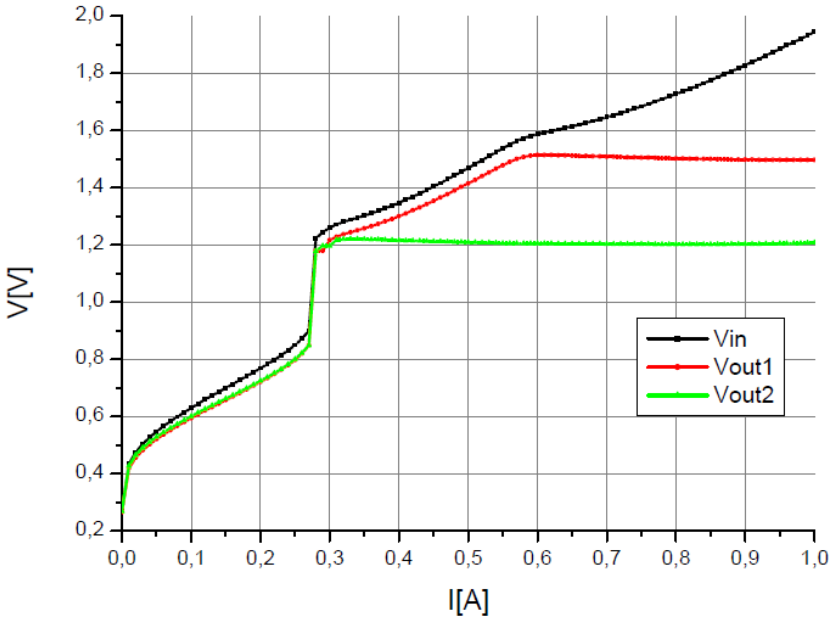

Fig. 5: Measuered IV characteristics of two parallel placed Shunt-LDO regulator with different output voltage.

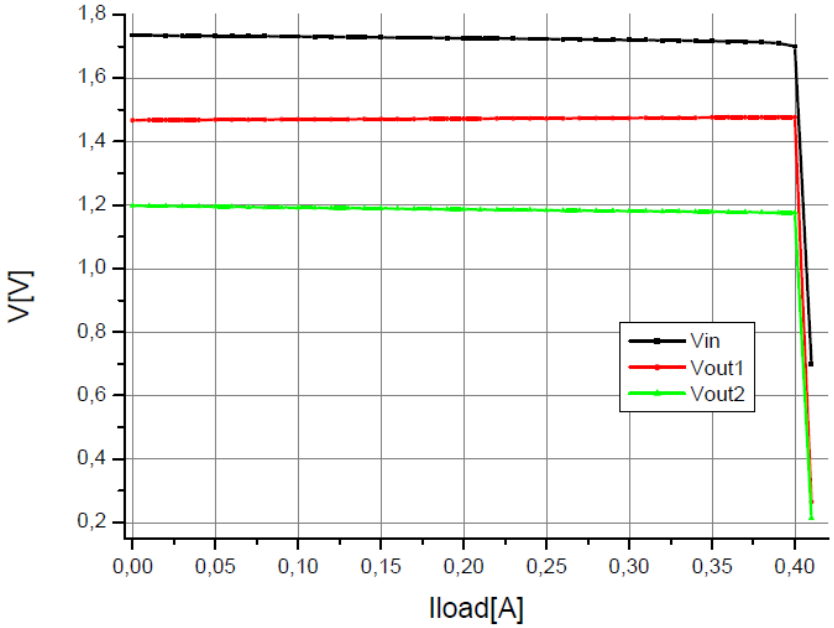

Fig. 6: Measurement of load regulation performance for two parallel placed devices.

In Fig. 7, the shunt current distribution between two regulators is measured at an input current of 1 A fed to the input of both regulators. One regulator generates a fixed output voltage of 1.2 V whereas the output voltage of the other regulator is swept from 1.2 to 1.5 V. The shunt current changes only about 6 mA in every regulator which corresponds to 1.2% of the shunt current flowing through the regulator at equal output voltage potential.

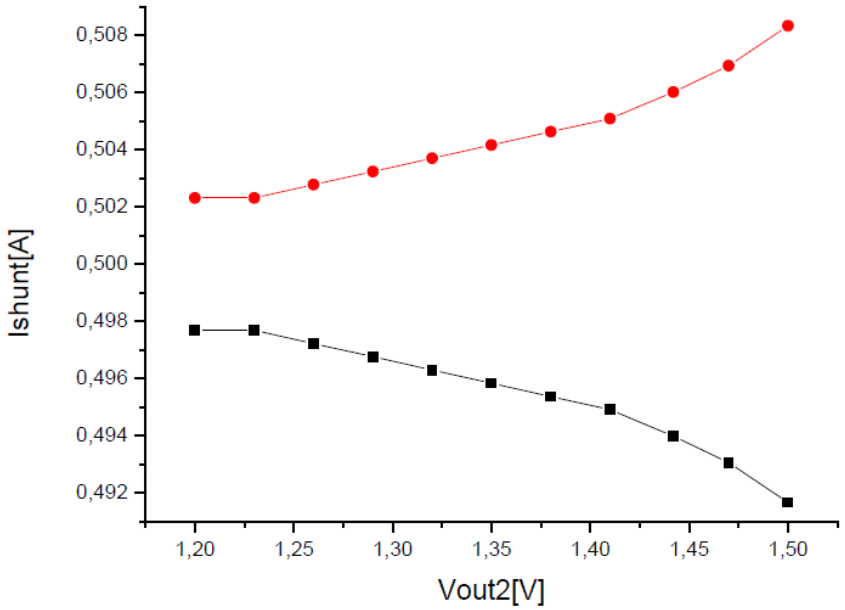

Fig. 7: Measured shunt current distribution with respect to output voltage difference.

An oscilloscope screenshot showing the load transient response of the regulator is found in Fig. 8. A load current pulse of 150 mA is applied to a Shunt-LDO regulator which leads to an output voltage change of about 10 mV (curve 2). This is equivalent to the output impedance of 60 m□ which has been measured in the static case in Fig. 6.

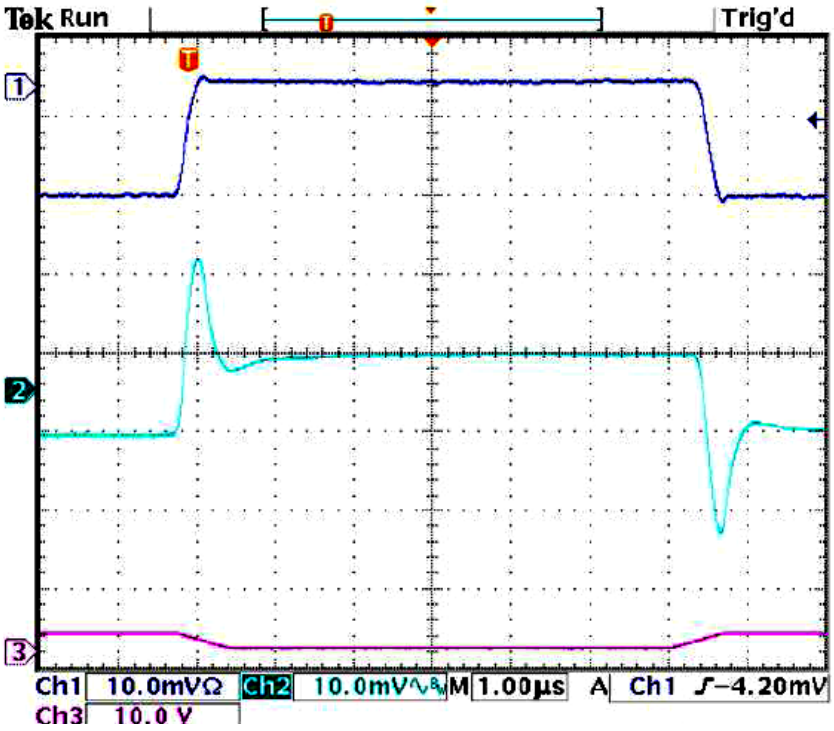

Fig. 8: Load transient behavior for a load pulse of 150 mA.

The shunt current distribution during power-up of two parallel operating regulators with different reference voltage is shown in Fig. 9. An unbalanced shunt current distribution arises when the output voltage of one regulator reaches the referenced output voltage level whereas the other is still lower than the referenced output voltage level. More current is flowing through the regulator which is already saturated and generates the smaller output voltage. As soon as both regulators have reached the nominal output voltage level the shunt current distribution improves and becomes balanced again.

This unexpected behavior understood and is caused by the offset of amplifier A2 which is used in the current mirror in Fig. 1. The offset of the amplifier leads to different *VDS* voltages at transistor M1 and M2 which influences the current mirror aspect ratio when M1 and M2 are in linear region. This is the case when the output voltage is lower than the referenced value. When the referenced level is reached, transistors M1 and M2 get saturated and the influence of the offset vanishes. A similar behavior could be demonstrated in simulation when an offset voltage of 20 mV is introduced to the amplifier A2. The shunt current distribution during power up can be improved when a special low offset architecture is used for amplifier A2. But still the available prototype does not exceed the maximum specified shunt current during power-up. In addition the observed behavior could be avoided completely, by choosing the same voltage reference during power-up and setting different voltages afterwards.

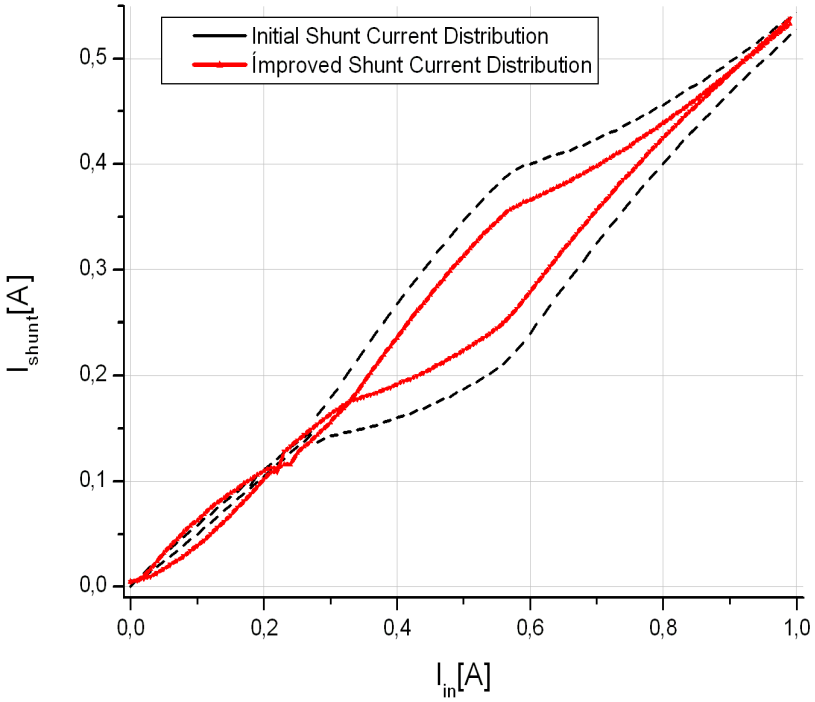

Fig. 9: Measured shunt current distribution during power-up.

The proposed Shunt-LDO regulation scheme allows robust operation of parallel placed devices which increases redundancy and reliability of serial powered systems. By use of this scheme additional flexibility is gained because parallel placed devices can generate different output voltages. The prototype study has proven the feasibility of the Shunt-LDO working principle and revealed the circuit part which is crucial for balanced shunt current distribution during startup. For use in a conventional voltage based powering scheme, the shunt part of the regulator can be switched off and the device can be used as an ordinary LDO regulator.

4. SHUNT REGULATORS FOR THE STRIP DETECTOR POWERING SYSTEM

In this section the three main shunt regulator architectures will be presented. Each is now available as fully custom circuitry. The two distributed options are named after their designers. The 'M' scheme designed by M. Newcomer is a distributed shunt with external feedback. The 'W' scheme designed by W. Dabrowski is a distributed shunt with the internal feedback. The stand-alone shunt regulator option employs the Serial Powering Interface chip (SPi).

The 'M' and the 'W" shunt regulators have been implemented in the ABCN-25 ASIC for readout of silicon strip detectors in such a way that they can be used alternatively. The ABCN-25 chip and the SPi chip have been designed in 0.25 μm process using layout hardening techniques. The block diagram and the mask layout of the ANCN-25 are shown in Fig. 10. The functional block diagram of the SPi chip is shown in Fig. 11.

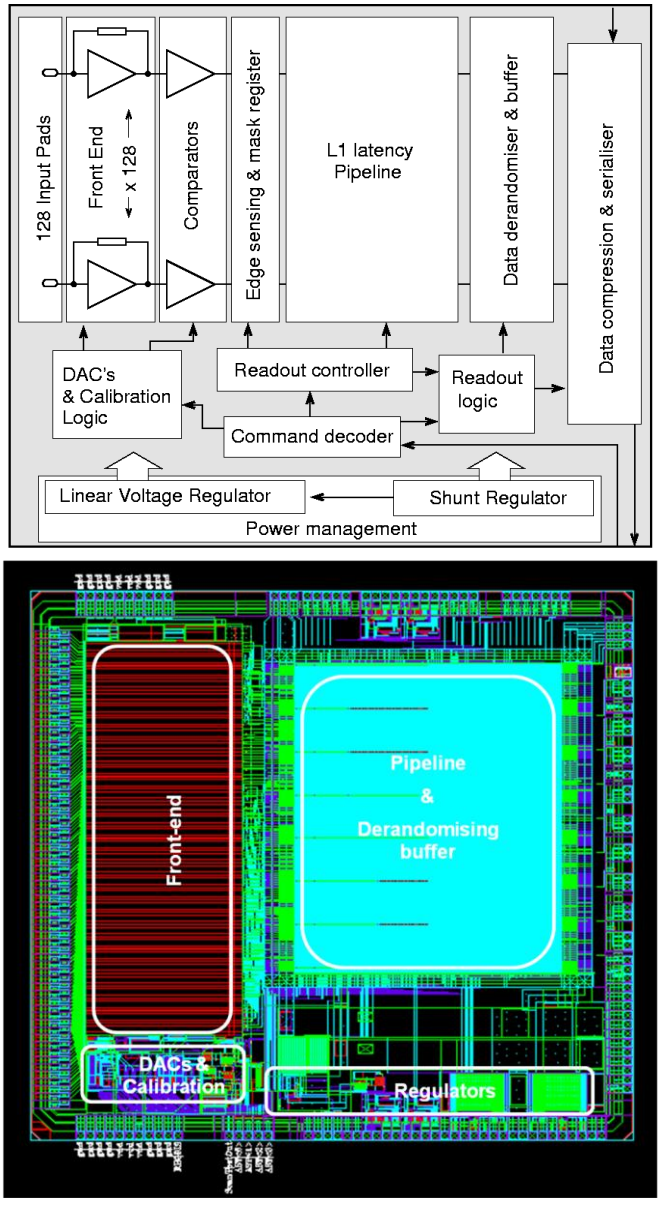

Fig. 10: Block diagram (top) and mask layout (bottom) of the ABCN-25 ASIC.

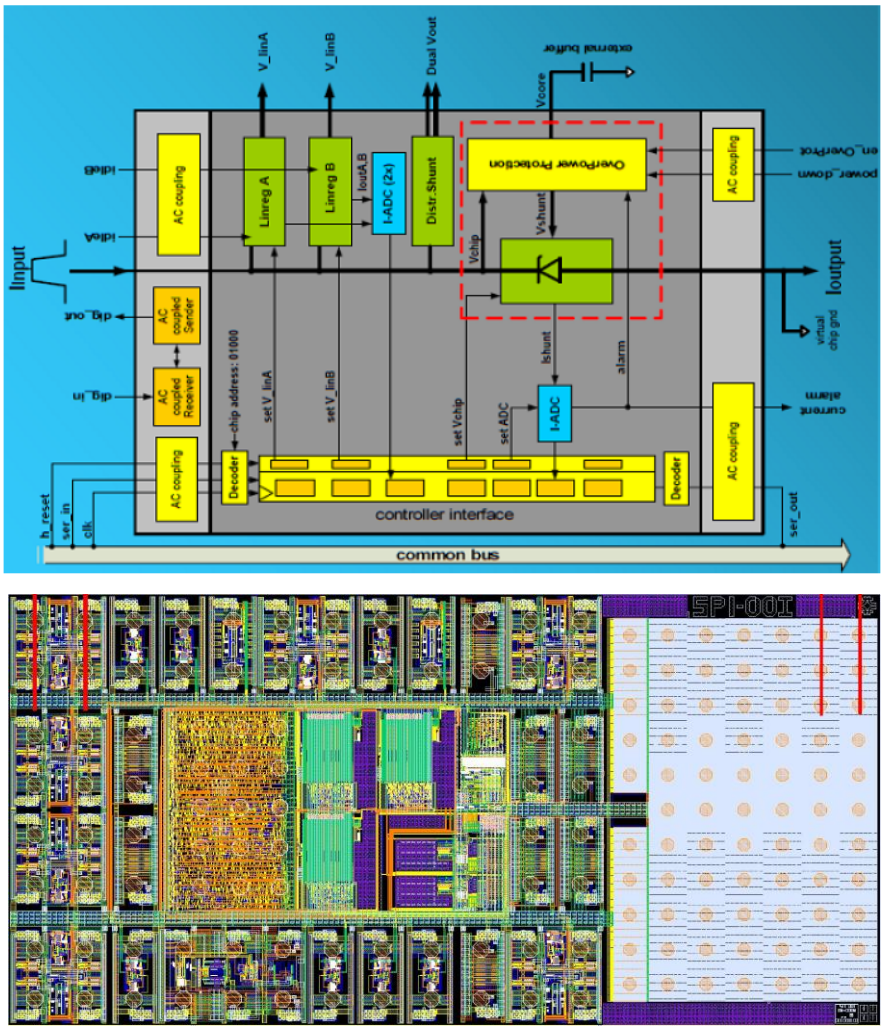

Fig. 11: Block diagram of the SPi ASIC (top) and mask layout (bottom) of the SPi ASIC. The chip is designed to be bump bonded. The bonding area can be seen on the right-hand side of the mask layout.

4.1. "W" SHUNT REGULATOR

This scheme utilizes one complete shunt regulator within each read-out chip. The scheme is tempting because it does not require any external shunt regulation components. A classical design of a shunt regulator consists of a voltage reference, op-amp and shunt transistor. This design cannot work at all in the case of many shunt regulators connected in parallel. There are some voltage drops along the power lines on the hybrid and also the voltage references cannot be perfectly matched because of random variations of the manufacturing process parameters. These effects would result in small number of chips shunting all the shunt current. The special design to overcome this difficulty is explained by the conceptual diagram shown in Fig. 12.

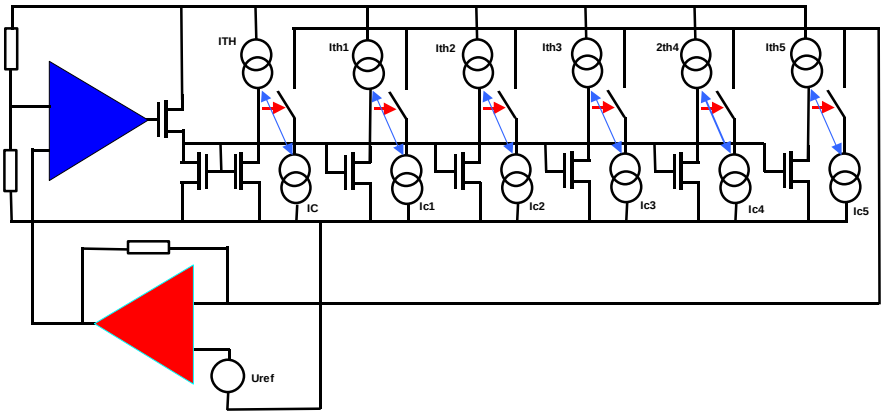

Fig. 12: Conceptual diagram of the 'W' scheme shunt regulator present in ABCN-25.

The shunt transistor is a P-MOS and its current is sensed and compared with six different current references. There is a trans-resistance amplifier which adjusts the reference voltage of the shunt op-amp. If the shunt current goes above one of the reference currents, the corresponding correction current source gets connected to the input of the trans-resistance amplifier thus adjusting the set-point voltage of the shunt regulator and the shunt current. One of the reference currents provides over-current functionality while the five others serve for shunt current redistribution within the hybrid during start-up. The 'W' scheme considers huge decline in current consumption of the ABCN-25 to be an accidental situation at which over-current protection should be activated. The shunt transistor is rather large for improved reliability.

The effectiveness of this circuit has been verified on a dedicated test board on which four ABCN-25 chips are powered, activated and transmitting data. Current monitors are added in the power distribution lines to measure the current of each ABCN-25 individually, whereas the power source is set in the current source mode. In Fig. 13, the voltage shunt operation with the four internal shunt devices in parallel is demonstrated, with the test board equipped with four ABCN-25. The voltage is limited below 2.8 V when the current on the board is forced well above the nominal current of 800 mA at 2.7 V. The additional current is derived through the shunt elements, as shown in Fig. 14. The currents per each ABCN-25 are showing the expected behaviour: looking at the chip ABCN0, the current in the shunt device is increasing according to the source current, then it gets limited to approximately 80 mA. When increasing the source current, the excess current is passing through the shunt devices of ABCN2 and ABCN1, up to the same limit of around 80 mA, finally it gets through the shunt device of ABCN3.

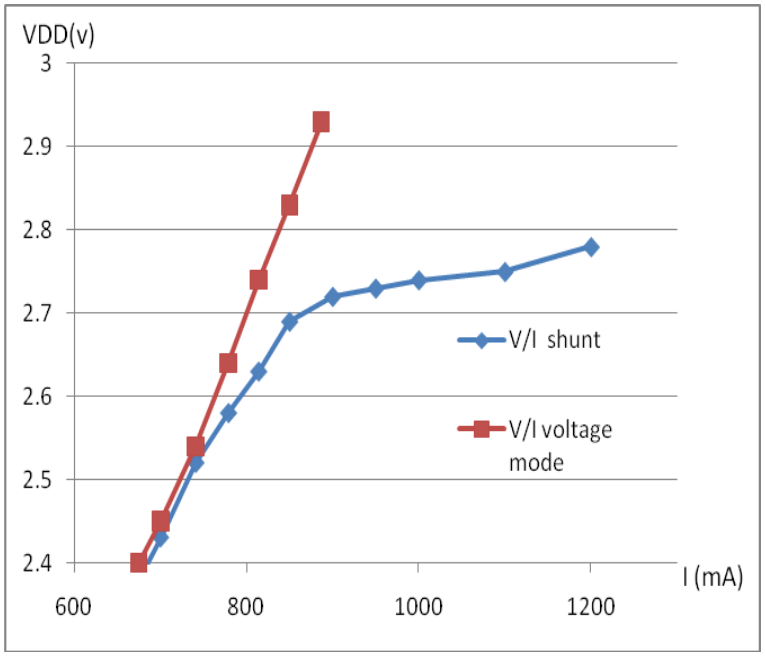

Fig. 13: Voltage versus current on the four ABCN-25 test board. Squares: V versus I with the power supply set as a voltage source. Diamonds: V versus I with the internal shunt enabled, and the power supply as a current source.

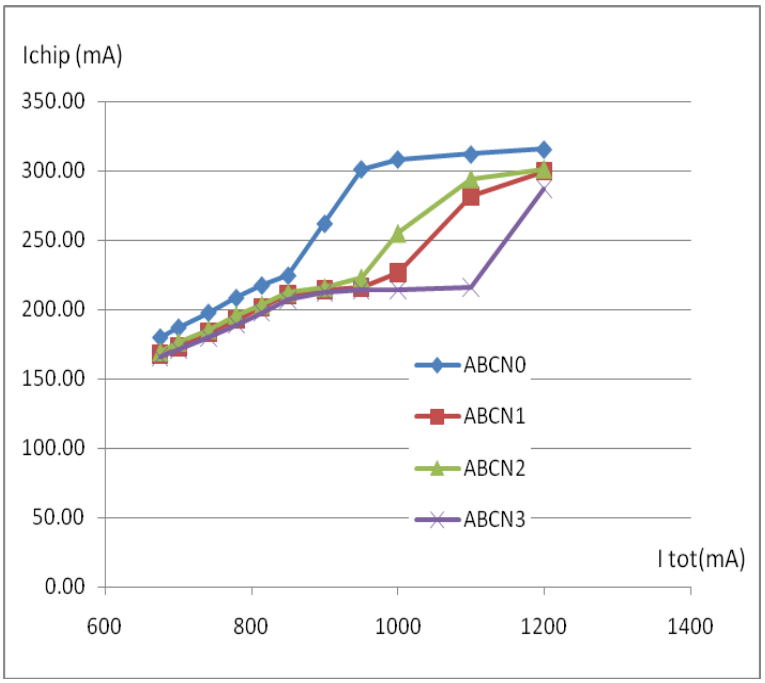

Fig. 14: Current distribution per ABCN-25 chip versus total current, internal shunt enabled.

4.2. "M" SHUNT REGULATOR

The schematic diagram of the distributed shunt devices with an external feedback control is shown in Fig 15. The external shunt control line drive the shunt elements distributed in ABCN-25 chips connected in parallel.

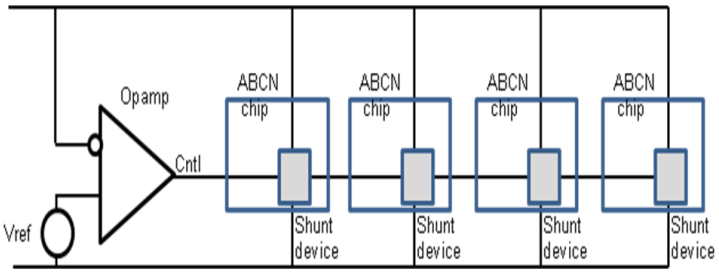

Fig. 15: Conceptual schematic diagram of the shunt regulator with auxiliary error amplifier.

In Fig. 16, the voltage shunt operation with the four shunt devices in parallel is shown, with the test board equipped with 4 ABCN-25. The voltage is limited slightly below 2.5 V when the current on the board is forced above the nominal current of 700 mA at 2.45 V.

The additional current is derived through the shunt elements, as shown on Fig. 17. The current in excess is reasonably distributed across each ABCN-25 shunt device. As expected, the degenerated current mirror circuit controlling the gate of the large shunt transistor helps to limit the difference of current, which may result from different transistor parameters. It avoids that one chip takes the majority of the excess current.

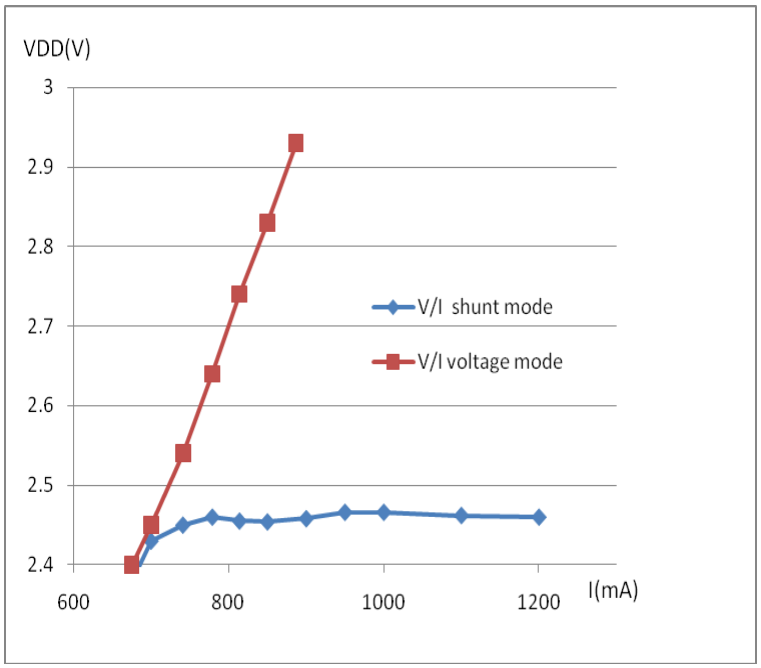

Fig. 16: Voltage versus current on the four ABCN-25 test board. Squares: V versus I with the power supply set as a voltage source. Diamonds: V versus I with the distributed shunt enabled, and the power supply set as a current source.

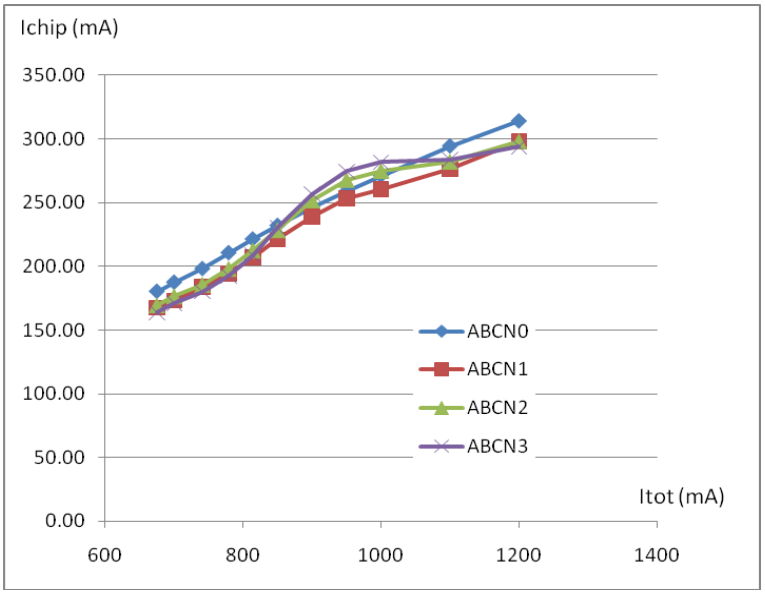

Fig. 17: Current distribution per ABCN-25 chip versus total current, distributed shunt enabled.

4.3. SERIAL POWERING INTERFACE CHIP

Serial powering interface chip is a versatile chip designed by M. The idea of the chip is to provide an universal solution for serial powering. It contains linear regulators, LVDS buffers, dual output current limited op-amp for the 'M' control scheme, its own shunt regulator with selectable output voltage as shown in Fig. 11.

The performance of the SPi chip has been evaluated using a dedicated test board. Figures 18 and 19 shows example characteristics of the programmable shunt regulator and the programmable liner regulator respectively. The test results confirm correct functionality of the chip. Furthermore, functionality of the SPi chip has been demonstrated by supplying from it a hybrid comprising twenty ABCN-25 readout ASICs.

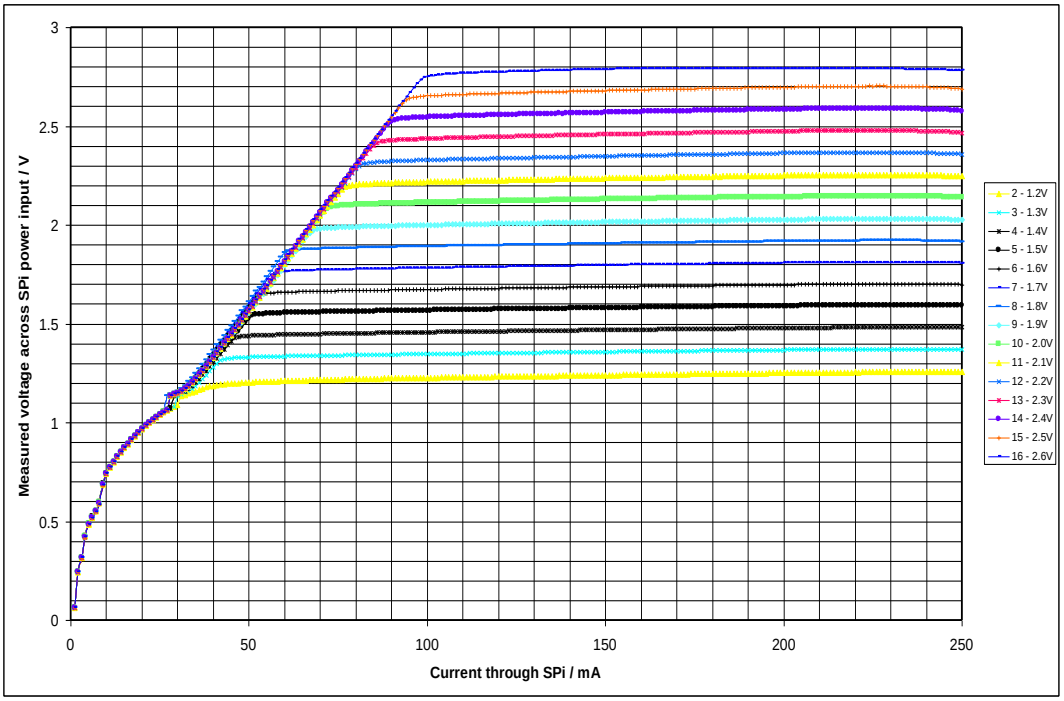

Fig. 18: Output characteristics of the shunt regulator for the output voltage programmed from 1.2 V to 2.8 V.

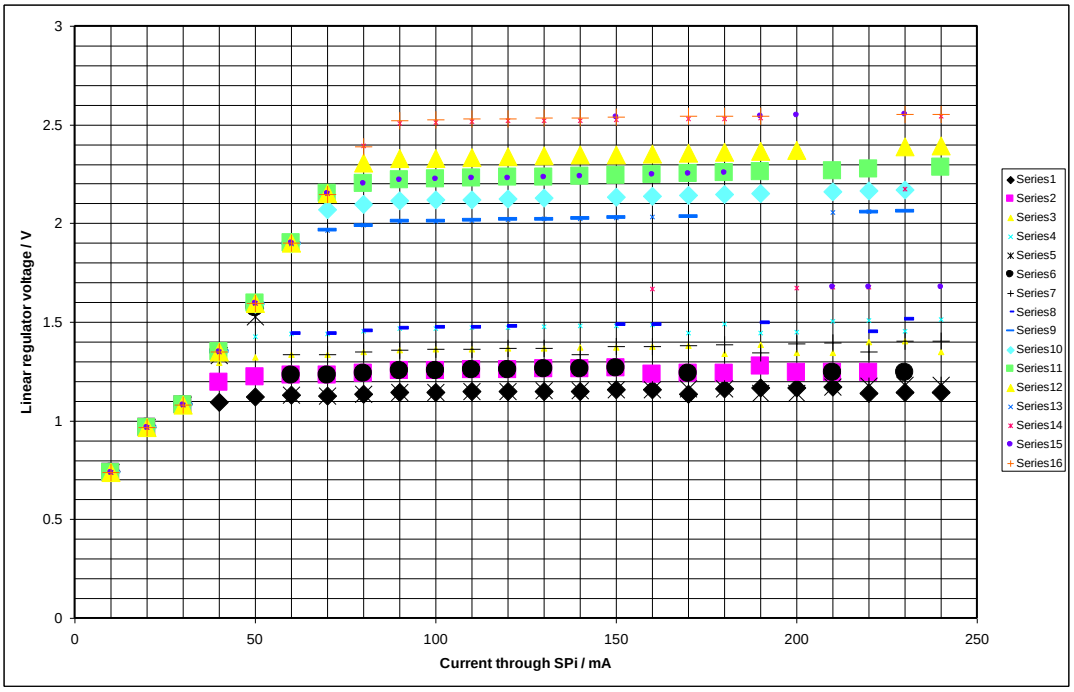

Fig. 19: Output characteristics of the linear regulator for output voltages programmed from 1.1 V to 2.5 V.

5. CONCLUSIONS

The three options of the custom-designed shunt regulators have been fully worked out and the prototype integrated circuits have been manufactured and fully evaluated. The development of serial powering system and its shunt regulators goes in parallel with development of the concepts and prototypes of the silicon strip detector modules using ABCN-25 readout ASICs. Full size silicon strip modules have been powered successfully using different options of the developed shunt regulators. No degradation of noise performance has been observed compared to if the modules were powered in the voltage mode.