SLHC-PP

DELIVERABLE REPORT

EU DELIVERABLE: 8.2.3

Document identifier:	**SLHC-PP-8.2.3-1133544-v1.0**
Contractual Date of Delivery to the EC	**End of Month 36 (March 2011)**
Actual Date of Delivery to the EC	**23/3/2011**
Document date:	**23/3/2011**
Deliverable Title:	**Full-scale super-module with custom serial powering circuitry**
Work package:	**WP8: Tracking detector power distribution**
Lead Beneficiary:	**AGH**
Authors:	**W. Dabrowski, J. Matheson, G. Villani,**
Document status:	**Released**
Document link:	https://edms.cern.ch/document/1133544/1

History of Changes

Version	Date	Comment	Authors
1.0	23/03/2011	Released	W. Dabrowski

The Preparatory Phase of the Large Hadron Collider upgrade (SLHC-PP) is a project co-funded by the European Commission in its 7th Framework Programme under the Grant Agreement n° 212114. SLHC-PP began in April 2008 and will run for 3 years.

TABLE OF CONTENTS

1. EXECUTIVE SUMMARY

The first serially powered full-scale silicon strip detector super-module, called stavelet, has been built using custom ASICs, custom serial powering circuits, and a custom current source. The silicon strip detectors assembled in the stavelet are read out by eight hybrids powered serially, each one comprising twenty 128-channel ABCN-25 readout ASICs, resulting in a total number of 160 readout ASICs powered through a single set of cables. This should be compared to the silicon strip detector modules used in the current ATLAS Semiconductor Tracker with twelve readout ASICs powered through an individual set of cables. Thus, more than 10-fold reduction of the cable count for a given number of silicon strips have been achieved in the developed prototype.

The stevelet project could be realized thanks to the concept of serial powering and components needed for such a system, which have been developed in the frame of work package WP8. The stavelet project has been developed by the ATLAS Inner Detector Upgrade community, which is much wider than the SLHC-PP collaboration. Through a very close collaboration between the SPLC-PP members and other ATLAS Upgrade groups the serial powering concept has been integrated into the stave concept along with all other critical aspects, like sensor design, overall readout scheme, mechanical and thermal design of the stave as a building block of the future silicon strip tracker. The silicon strip detectors are read out by the ABCN-25 ASICs, which include dedicated circuitry for the serial powering. A fast real-time bypass circuit protects against failure of the serially powered chain of hybrids and a slow control system allows to switch off and bypass individual hybrids in the serial chain.

Experimental results confirm that the modules powered serially can be read out without degradation of noise, compared to individual module performance. It has been demonstrated that the stavelet can be operated safely and without impairing performance also in configurations when individual hybrids need to be switched off and bypassed. This demonstrates that switching hybrids on or off is possible with serial powering, addressing main concerns about robustness and safety of the serially powered chain of modules against various possible failure modes. Further stavelets will be constructed and the experience gained will be used to design a prototype of 24-module double-sided stave for the tracker upgrade. The conclusions from this work will remain valid for future designs using new generation of front-end ASICs developed in 130 nm CMOS technology.

2. INTRODUCTION

The concept of serial powering of the modules assumes that the building block of the future silicon strip detector tracker will be a relatively large object comprising up to 24 modules mounted on two sides of a carbon fiber support, with signal and power cables on each side [1], [2]. Each module is based on a silicon microstrip detector, of 96×96 mm^2, with 1280 strip, 2.4 mm long, arranged in four columns. Two readout hybrids are glued to each detector, each hybrid carrying two columns of readout ASICs, which will be powered serially. Therefore, in order to demonstrate that such a design is feasible a prototype of a reasonable size has been built. The present 4-module prototype termed stavelet prototype has been built using the prototype silicon strip detectors and the 128-channel ABCN-25 readout ASICs manufactured in a 0.25 μm CMOS process.

It should be noted that the design and construction of the stavelet prototype involves a much wider range of technologies than those specific for the serial powering, covered by the SLHC-PP project, and much wider community besides the members of the SLHC-PP consortium involved in the work package WP8.

Within the ATLAS Inner Detector Upgrade community the work has been already started to design a 256-channel readout ASIC in a 130 nm CMOS process, which will allow to place the readout ASICs in one column and reduce the area and material budget of the hybrid accordingly. Also, the new readout ASIC will need lower power supply voltages and it is expected to consume less current. Those aspect do not change, however, the critical issues of the serial powering and the designs of hybrids, bus cables, protection and AC-signal coupling circuits will be based on the experience gained with the present prototype.

3. STAVELET PROTOTYPE

The first stavelet has been assembled at the STFC Rutherford Appleton Laboratory, using modules provided by Liverpool University [6]. This is a test vehicle, to examine options for: grounding and shielding, bus cable layout, and serial powering. A photograph of the prototype is shown in Fig 1. Four silicon strip detector modules, each one read out by two hybrids equipped with ABCN-25 chips are mounted on a carbon fiber frame. The eight hybrids are powered through a serial chain. Therefore each hybrid needs a shunt regulator to stabilize the supply voltage for all ABCN-25 chips on the given hybrid. Various options for realization of the shunt regulation and the dedicated designs have been described in the deliverable report 8.2.2. There are two shunt regulation options within the ABCN-25 [4], [5], termed M-shunt and W-shunt. The M-shunt option uses two shunt transistors in each ASIC, controlled by a voltage from an external circuit. The W-shunt option uses both shunt and control circuitry within the ASIC itself. Shunt regulation may also be implemented outside the readout ASIC, using an additional Serial Powering Interface (SPI) ASIC [3].

The Power Protection Boards (PPB) are visible along the top edge of the stavelet. Each PPB carries a connector, which gives access to the hybrid power lines and the two M-shunt control lines. This allows the use of power regulation plug-in PCBs for testing different serial powering options. A multi-drop bus runs below the PPBs to allow addressing of the dedicated Serial Powering Interface (SPI) chip, which is used in one of the option for implementation of shunt regulators on the readout hybrids. Along the bottom edge of the stavelet, add-on PCBs carry Buffer Control Chips (BCC) for each hybrid. These multiplex the outputs from the two columns of ABCN-25s onto a single bus cable line pair. They also implement a clock multiplier to derive an 80MHz clock for the ABCN-25 readout from 40 MHz LHC bunch crossing clock.

Serial powering of a chain of hybrids requires a constant current power supply. This must supply a voltage equal to the sum of the individual hybrid supply voltages, plus any voltage drops along the cables. It must be able to deliver a stable current equal to the maximum expected demand for a single hybrid. A custom current source has been developed and used for the performed tests of the stavelet.

The stavelet structure includes also adapters that allow powering individual modules through the DC-DC converters, which have been developed in the frame of task 8.1 of the SLHC-PP project.

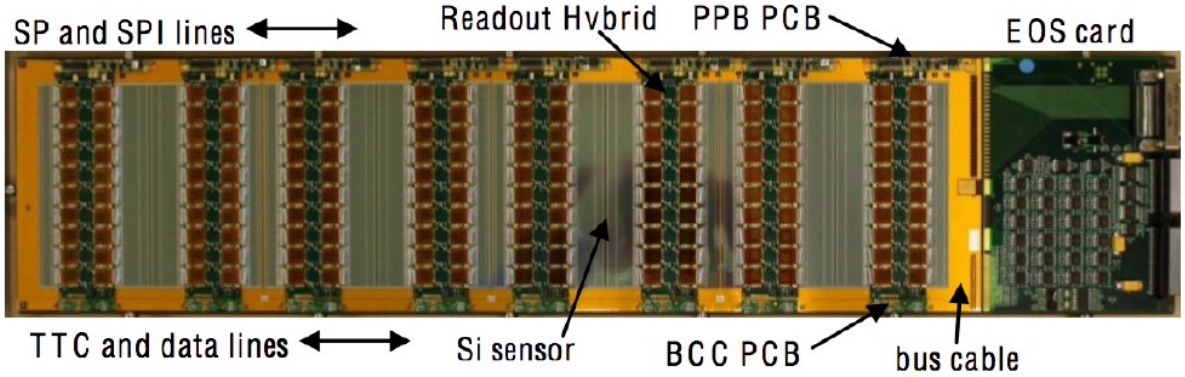

Figure 1. Photograph of the 4-module stavelet with ABCN-25 readout and all circuits required for serial powering.

4. TEST RESULTS

In order to prove that the developed scheme of serial powering of silicon strip detector modules is suitable to be implemented in the upgrade tracker one has to demonstrate that: (1) serial powering does not introduce additional sensitivity of the modules to external system noise sources, compared to configuration with each module powered individually, and (2) the modules powered serially can be operated safely and possible failures of individual modules, which have to be taken into account, will not affect the operation of the entire chain.

The prototype stavelet was powered using the current source, with shunt regulation provided by the on-hybrid M-shunt circuitry and shunt transistors integrated in the ABCN-25 readout ASICs. Triggers were sent to the ABCN-25s, using the on-chip calibration system to generate input charges of 1.5, 2.0 and 2.5 fC. Gain and ENC were measured for each channel over the 16 columns of chips. Mean gain for each column lay in the range 104 – 107 mV/fC, cf. the design value of 110 mV/fC. The ENC plots are shown in Fig. 2. Whilst work continues to optimize the stavelet noise performance, it is already within the ATLAS Tracker Upgrade specification of 750 RMS electrons. The performance of the ASICs is very similar to that measured on individual modules. Small anomalies were seen; Hybrid 2 Column 0 shows some dead channels and Hybrid 3 Column 1 shows a faulty calibration line. Zero noise appears on a few dead channels. These problems can be easily eliminated during production by ASIC screening. Channels with noise near 400 ENC have failed bonds to the sensor strips.

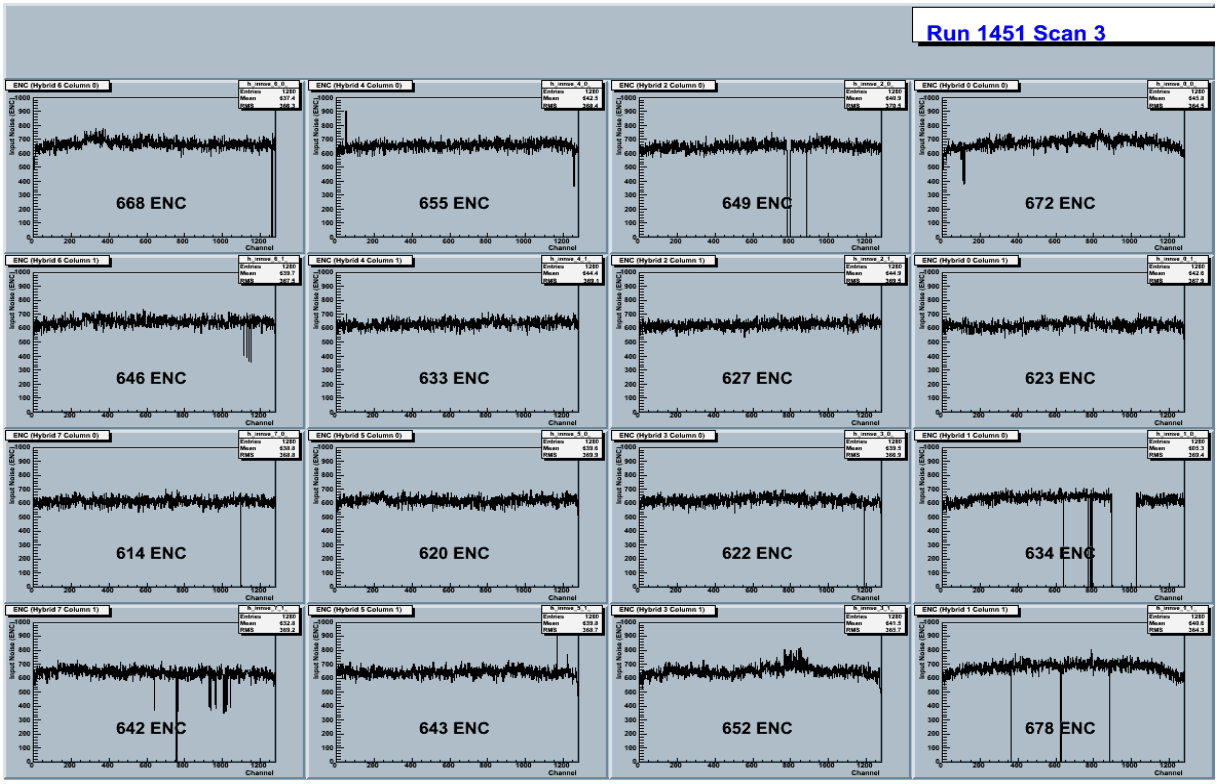

Figure 2. Noise measured for the entire stavelet powered serially. Each plots shows the Equivalent Noise Charge (ENC) across 1280 readout channels, i.e. 10 ABCD-25 chips, and the mean values of ENC.

A concern with the serial powering scheme is that an open-circuit failure of a hybrid may cause the failure of an entire chain. It is also desirable to be able to turn individual hybrids off and on remotely. Therefore an alternative current path in parallel with each hybrid is needed, with the possibility of both local, autonomous activation and remote activation. These functions are provided by the power protection circuitry, which is currently implemented as small PPBs. Figure 3 shows infrared images of the stavelet in operation. The hot rectangles corresponding to ABCN-25 chips, the main source of power dissipation on the hybrid, are clearly visible. The upper image shows all eight hybrids powered, middle and lower images show every second hybrid powered and every second one bypassed, alternatively, using the PPB. As hybrids are turned off by the DCS system, the ASICs cool down and heat dissipation instead becomes visible at the position of the bypass circuitry. Gain and ENC were measured for the stavelet, running every second hybrid only. Gain was unaffected, whilst a small reduction in noise was seen, which could be attributed to a lower overall temperature of the hybrid.

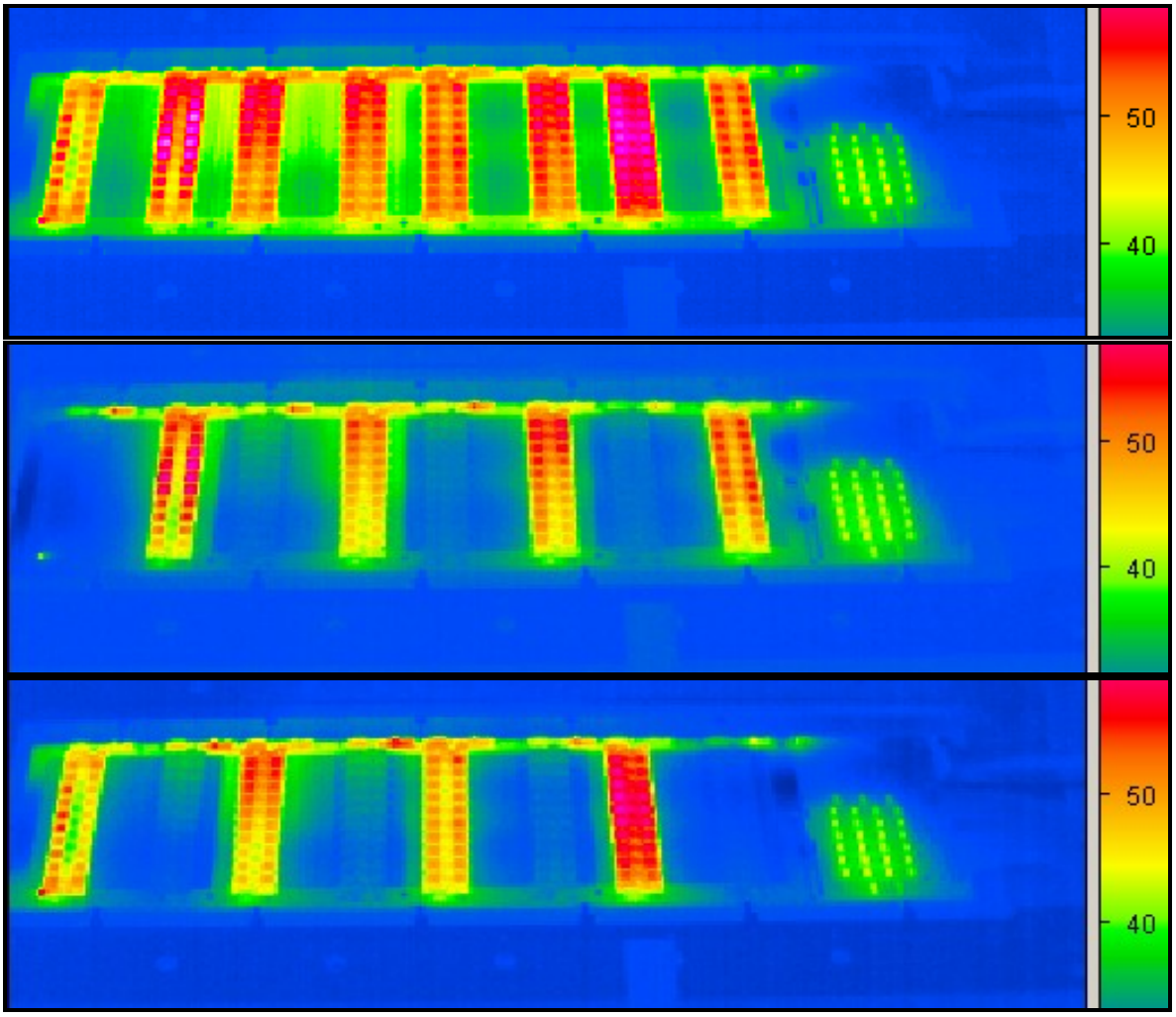

Figure 3. Infrared images of temperature distribution on the hybrid for all hybrids powered (upper), odd hybrids bypassed and even hybrids powered (middle) and odd hybrids powered and even hybrids bypassed (lower).

5. CONCLUSIONS

The concept of serial powering of silicon strip detector modules has been demonstrated for the prototype stavelet designed and built by the ATLAS Inner Detector Upgrade community, using the custom components developed within the SLHC-PP framework and by other members of the ATLAS Upgrade Community. The extensive testing of the stavelet provide a solid proof of principle that the serial powering is a feasible and efficient option to be used in the Inner Detector Upgrades.

Although a new generation of front-end ASICs for the phase2 upgrade silicon trackers is under development using 130 nm CMOS process the experience gained with serial powering of the stavelet based on ABCN-25 front-end chips and the conclusions from this work are fully applicable to future designs.

6. REFERENCES

[1] M. Weber, Power distribution for SLHC trackers: Challenges and solutions, Nucl. Instr. and Meth. A, Vol. 592 (2008), 44

[2] E.G. Villani, C. Haber, R. Holt, P. Phillips, M. Tyndel, M. Weber, "Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade", Nucl. Phys. B (Proc. Suppl.), Vol. 197, Issue 1 (2009), 250.

[3] T. Tic, P. W. Phillips, M. Weber, "Performance and Comparison of Custom Serial Powering Regulators and Architectures for SLHC Silicon Trackers", Proceedings of the Topical Workshop on Electronics for Particle Physics TWEPP-09, Paris, France, CERN-2009-006.

[4] F. Anghonolfi, W. Dabrowski, N. Dressnandt, J. Kaplon, D. La Marra, M. Newcomer, S. Pernecker, K. Poltorak, K. Swientek, "Performance of the ABCN-25 readout chip for the ATLAS Inner Detector Upgrade", Proceedings of the Topical Workshop on Electronics for Particle Physics TWEPP-09, Paris, France, CERN-2009-006.

[5] W. Dabrowski, F. Anghinolfi, N. Dressnandt, M. Dwuznik, J. Kaplon, D. La Marra, M. Newcomer, S. Pernecker, K. Poltorak, S. G. Sevilla, K. Swientek, "Design and Performance of the ABCN-25 Readout Chip for the ATLAS Inner Detector Upgrade", Proceedings of the 2009 Nuclear Science Symposium and Medical Imaging Conference, Orlando, Florida, USA, October 2009.

[6] J. Matheson, Progress and advances in Serial Powering of silicon modules for the ATLAS Tracker Upgrade, J. of Instrumentation (2011), C01019,